Radio Shack®

Technician Series Diagnostics Software

TRS-80®

MODEL III/4/4P

DIAGNOSTICS MANUAL

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Diagnostics Update
Radio Shack Dept. #0220
400 Atrium, One Tandy Center
Fort Worth, Tx. 76012

Dear Customer,

To help keep you up to date on the current versions of Diagnostics programs, we are offering a computer bulletin board to notify you of updates to the Diagnostics programs. You will then have the option to have your current diskette upgraded to the latest version.

New releases will be for corrections to old programs, enhancements to current programs, or new programs added to the diskette.

If you decide to upgrade your diskette, you must send in your original master diskette, with the "Technican Series Diagnostic Software" label, and the fee for the upgrade. The fee for the upgrade will be $30.00 in US dollars in a cashiers check or money order and should be payable to 'RADIO SHACK #0220, Diagnostics Update'. For your protection, do NOT send cash.

The computer bulletin board will include the current version numbers and dates of all diagnostic packages in this program. Be sure to check the part number & date of your diskette against the listing to avoid mistakes.

The phone number for the computer is (817)-338-2378. In response to the question 'Login:', respond 'diag' in lowercase. This bulletin board can be used at 300 or 1200 baud. It requires 8 bit words, 1 stop bit, and no parity. Messages can be left to the operator by responding 'help' to the 'Login:' question.

The address to send the ORIGINAL copy of the diagnostic diskette along with the update fee is:

Diagnostics Update
Radio Shack Dept. #0220
400 Atrium, One Tandy Center
Fort Worth, Tx. 76012

Please include the the following form, or a copy, with each request.

Name _____

Title _____

Address _____

City, State Zip _____

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READ ME FIRST

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To take advantage of these services, you must do three things:

(1) Send in the postage-paid software registration card included in this manual immediately. (Postage must be affixed in Canada.)

(2) If you change your address, you must send us a change of address card (enclosed), listing your old address exactly as it is currently on file with us.

(3) As we furnish updates or "patches", and you update your software, you must keep an accurate record of the current version numbers on the logs below. (The version number will be furnished with each update.)

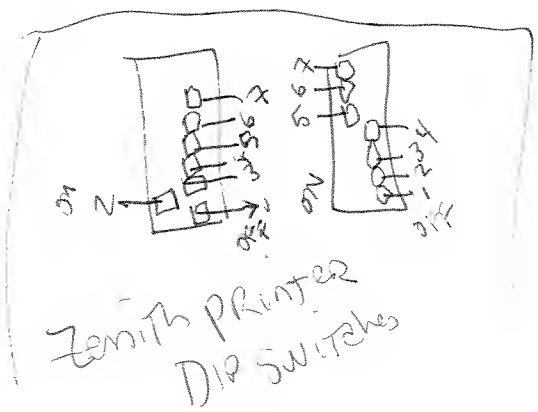
Keep this card in your manual at all times, and refer to the current version numbers when requesting information or help from us. Thank you.

APPLICATIONS SOFTWARE VERSION LOG

_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____
_____	_____	_____

OP. SYSTEM VERSION LOG

_____
_____
_____
_____
_____
_____



875-9242/2/28/83

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MODEL 4/4P ONLY

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IMPORTANT NOTICES:

This diagnostic software and manual has been written for TRS-8Ø™ computer owners who have a thorough understanding of electronics and computer circuitry. It is not written at a comprehension level for the beginner.

Radio Shack® will not be liable for any damage caused, or alleged to to be caused, by the customer or any other person using this diagnostic software or manual to repair, modify, or alter any TRS-8Ø™ computer in any manner.

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DMT Diagnostic Manual

BURNIN Diagnostic Manual

MEM6 Diagnostic Manual

DT1DIAG Diagnostics Manual

IOTEST Diagnostics Manual

FDCALG Diagnostic Manual

TDC Diagnostic Manual

DISKDG3 & DRV4M Diagnostics Manual

HDDIAG Diagnostic Manual

RS232 Diagnostic Manual

M4MEM &BD16K Diagnostic Manual

Preliminary Model 4/4P Diagnostic Manual

INTRODUCTION

These diagnostics are meant to be an aid in the troubleshooting of Radio Shack® TRS-8Ø™ computers. While they do a good job of testing the computer, the final test is the customer's programs. To test for every possible failure, no matter how obscure, is impossible.

This manual has been broken down into three sections; Model III only, Model 4/4P only, and all models. Programs in the all models section will run on any of our Model III, 4, or 4P computers, and are included on both diskettes. Model III only programs will only run properly on Model III's. Model 4/4P programs will only run properly on Model 4/4P's.

While the manual sections describe how to run the programs from the TRSDOS READY level, the diskette is organized into a 'menu tree' type structure. See Figures 1 & 2 for the current trees. The date above the main menu represents the version date of the diskette. If the user prefers, the menu function can be disabled by typing in 'AUTO' from the TRSDOS READY prompt. This will allow the user to execute the programs from the TRSDOS READY prompt. To list the programs on the diskette, use the 'DIR (INV)' command.

Diagnostics Coordinator
Technical Support

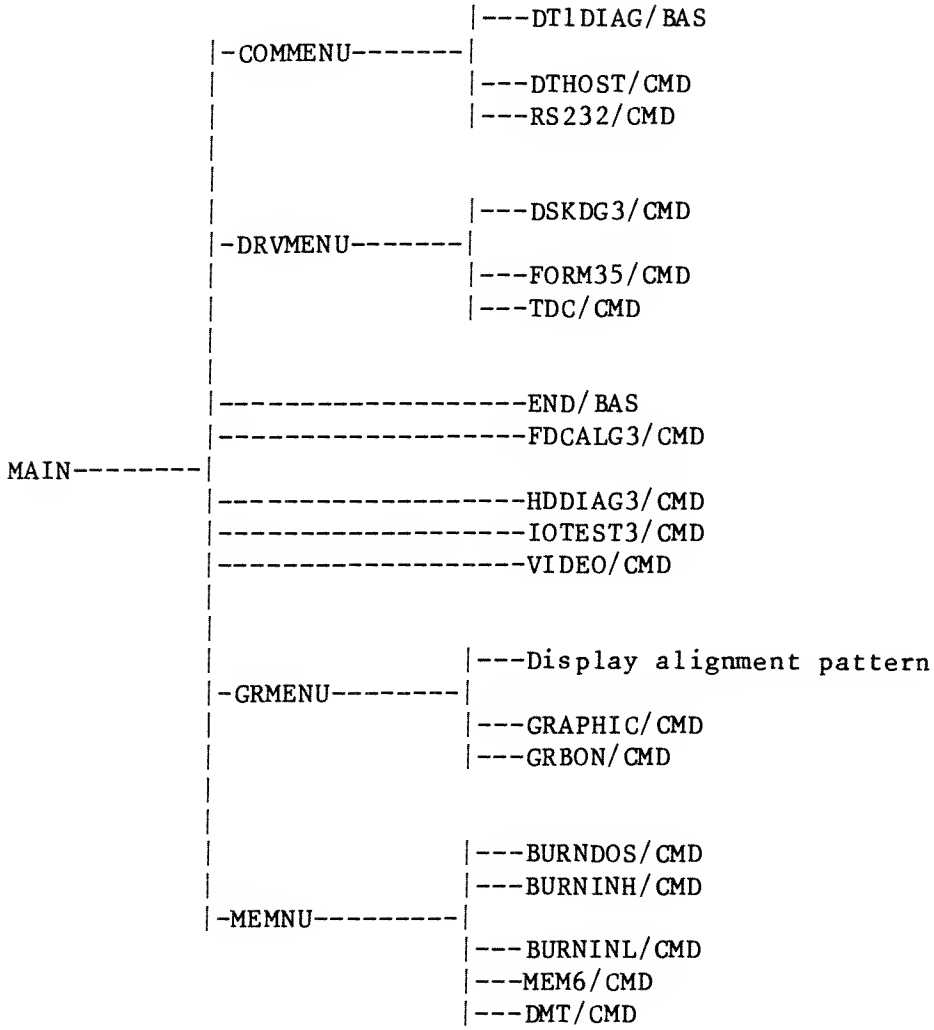

Figure 1
Model III tree

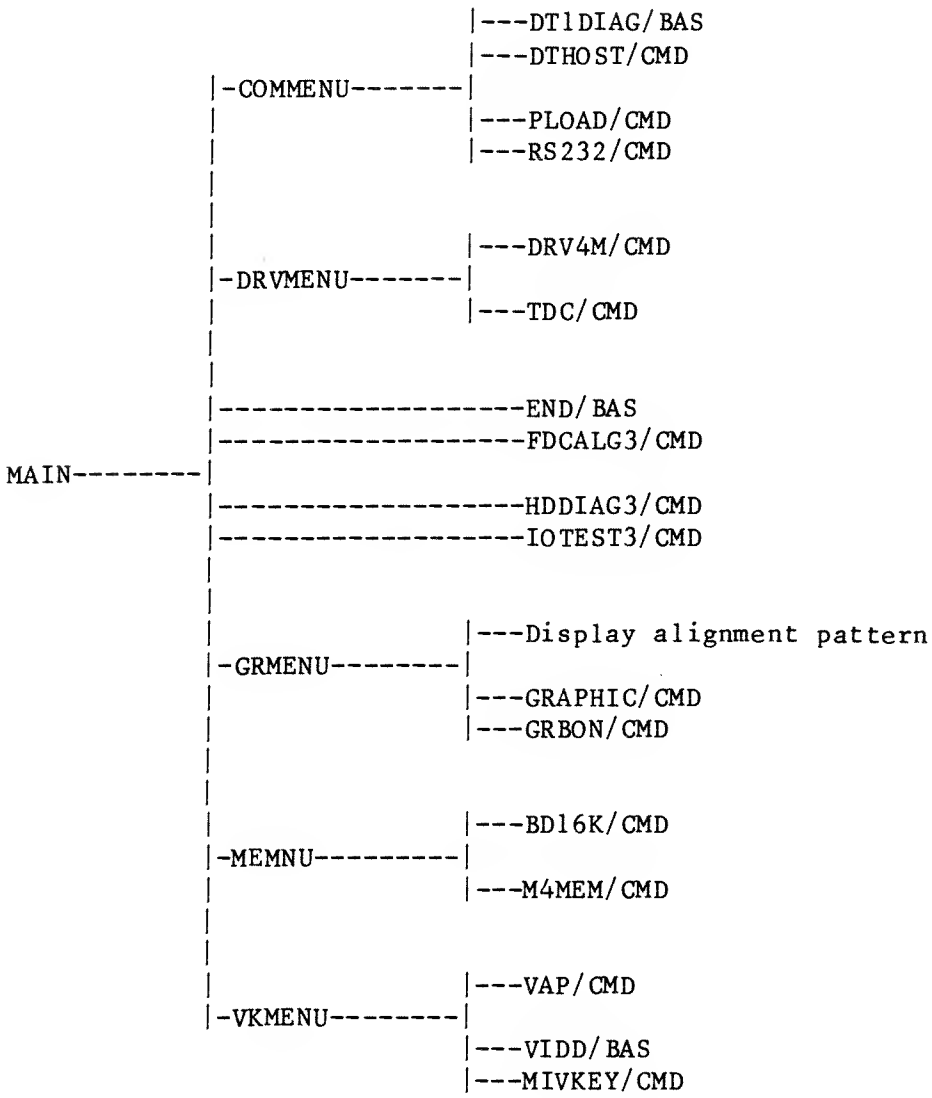

Figure 2
Model 4/4P tree

DYNAMIC MEMORY TEST
DMT

CHAPTER 1

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DYNAMIC MEMORY TEST

General description

The Dynamic Memory Test programs (DMT's) are designed to detect elusive memory problems that conventional memory tests may not find. This is accomplished by a program that relocates itself through the RAM, versus the conventional type memory test that stores, reads, and checks values in RAM. The DMT programs utilize the Z8Ø "LDIR" instruction to relocate, thus realizing a real-time, maximum memory transfer rate.

Features

Self-prompting user oriented software
Graphic program location/system memory size display
Escape from failure to operating system provided
Fast memory fault detection
Disk and tape versions
Allows all system memory configurations to be tested
Model I and III compatible.

LOADING AND EXECUTING DMT

For disk systems (Model I and III), place the diskette containing DMT in the system drive and type:

DMT <ENTER>

For non-disk systems, use the BASIC "SYSTEM" command to load DMT from tape.
NOTE: Systems with 4K RAM must use the tape version of DMT!!!!!

To load DMT tapes type:

SYSTEM <ENTER>

The system will respond with prompt:

*?

type:

*? DMT <ENTER>

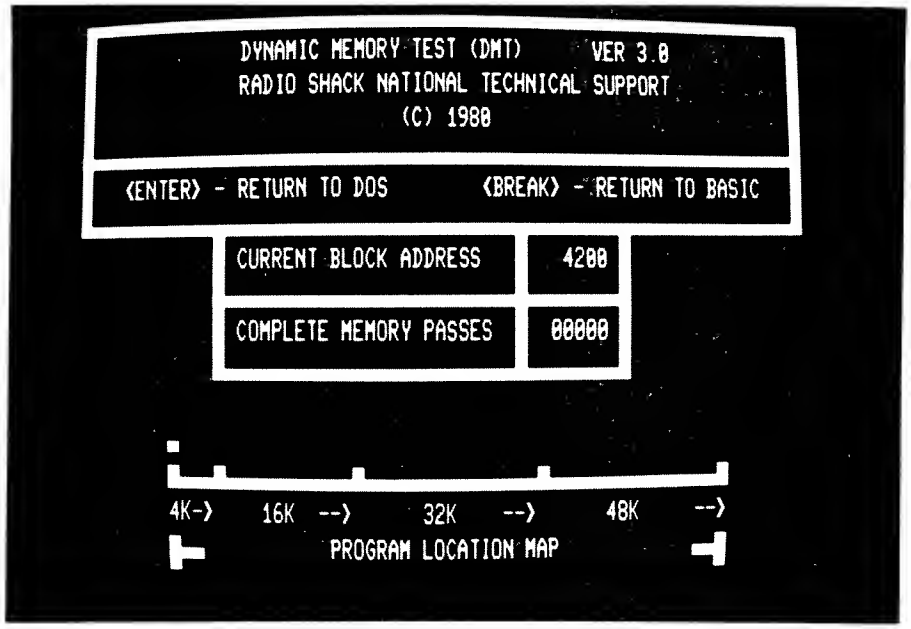
When loading is completed, the prompt will appear again. To execute program type:

*? / <enter>

During program execution, the user may return to the operating system (DOS or BASIC READY prompt) by depressing <ENTER> or <BREAK>.

DISPLAY FORMAT

Upon execution, the program will display the following screen format:



<ENTER> - RETURN TO DOS <BREAK> - RETURN TO BASIC line will be displayed unless an error is encountered. When an error is detected, it will flash the message:

********** ERROR! FAILURE HAS OCCURRED! **********

CURRENT BLOCK ADDRESS: Displays the current hex address of the 256 byte segment under test. Upon failure, this address will reflect the RAM area which caused the failure.

COMPLETE MEMORY PASSES: Number of times the program successfully relocated through the entire system RAM.

The "blip" position represents the programs latest successful load location. It also refects the amount of RAM in the system corresponding to how far it travels to the right.

The hash marks on the graph define the beginning of a new section of RAM (4K, 16K, etc.).

TRANSFERRING DMT TO DISK

Prepare the DMT (disk version) tape and use the Model III TRSDOS "TAPE" command:

Boot TRSDOS and type:
TAPE (S=T,D=D) <ENTER>

The program will prompt:
Cass?
Respond with "L".

When the program is completed, DMT/CMD will be listed in the drive directory.

If DMT is provided on diskette, use the "TAPE" command to make tape copies.

Boot TRSDOS and type:
TAPE (S=D,D=T) <ENTER>

ISOLATING BAD RAM WITH DMT

In typical applications, a system with a suspected memory problem should first be checked using a conventional type memory test. The advantage to using the conventional type test is that the actual faulty component will be listed upon detecting a failure. The disadvantage to conventional memory tests is that they often fail to find certain types of memory faults, i.e., a unit that will not properly execute programs may pass the memory test! DMT is highly successful in finding the cause of failure in this situation.

To isolate the defective component(s), run DMT. When a failure is detected, the Current Block Address will contain the address of the 256 byte area that caused the failure.

1. Using the memory map, determine which bank of RAM's the failure occurred in.

2. Remove one-half of the RAM's in the bank, and substitute known good RAM's in their place.

3. Run DMT again.

   A. If no failure occurs, then the faulty RAM is in the removed RAM's. Reinstall the suspect RAM's one or two at a time and re-run DMT. Repeat until installation of one RAM causes a failure. This will be the defective RAM.

   B. If failure occurs, then the faulty RAM(s) is one of the remaining original RAM's in the unit. Exchange these RAM's one or two at a time with known good RAM's, and re-run DMT. Repeat until exchange of one or more defective RAM's allows the test to run properly.

Use of this method will allow fast diagnosis of faulty RAM components.

NOTE: Occasionally, when a failure occurs at the boundary of two sets of RAM's, DMT may indicate the failure to be in the lower bank, when it is in the higher bank. Exchanging banks with a good set of RAM will aid in isolating the bank with the failure.

TECHNICAL DESCRIPTION

DMT consists of three modules:

Initialization: Upon loading and execution the stack is defined and fixed RAM subroutines and scratchpads are transferred to 4ØØØ-4ØA8. The screen format is printed, and then the relocatable module is transferred to 41ØØ. The initialization module then jumps to 41ØØ. Upon execution, the initialization routine is wiped out.

Fixed Ram (4ØØØ-4ØA8): Contains the following routines--
RST1Ø vector for print error
Error printing, keyboard scan
Hex to ASCII conversion
Get PC
Scratch RAM

4ØA9-4ØFF is reserved for stack usage.

Relocatable Module: A 256 byte routine that relocates itself through all available RAM, except the fixed RAM area.

Theory of Operation

Once initialized, the Relocatable Module (RM) begins at 41ØØ. The module loads Restart 1Ø instruction (ØD7H) in all memory above its end (256 bytes). The module then relocates itself up 256 bytes, jumps to its new location, and loads RST1Ø instructions in its previous location. With each jump, the RM checks to see if it has reached top of system memory or if it is in lowest memory, and takes the proper course of action if either is true. With each move the RM prints the address of the beginning of the next memory block it will attempt to relocate into.

A memory fault is detected when the RM jumps up to its next location and the machine code has been altered due to the fault. This will cause the RM to execute improperly, and in most cases, it will end up making a jump to an address outside the module's code. Since the module had previously loaded restart 1Ø vectors in all memory outside itself, it will jump to the RST1Ø vector, which was initialized to point to the print error routine. The error message will be printed, and the block RAM address where the error occured will be maintained on the screen for analysis.

DMT will detect illusive memory failures that conventional memory tests overlook due to the fact that is an actual program executing at high speed (using Z8Ø LDIR instruction), rather than just poking and checking memory contents. It is also prone to detecting memory that drops bits, since after each block transfer is executed, there is a programmed delay before the new block code is executed.

MEMORY MAP - HEX BLOCK ADDRESS VS. RAM BANK

4ØØØ-4FFF	4K RAM BANK (4K Model I CPU) (4K Model III, U-7-U14)	
4ØØØ-7FFF	1st 16K RAM bank, "16K System"	(Model I CPU) (Model III U7-U14)
8ØØØ-BFFF	2nd 16K RAM bank "32K System"	(Model I EI, Z9-Z16) (Model III, U25-U32)
CØØØ-FFFF	3rd 16K RAM bank 48K System"	(Model I EI, Z1-Z8) (Model III, U43-U5Ø)

MEMORY BURN IN TESTS

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MODEL III MEMORY TEST - BURNIN/CMD

General Description

The Model III Memory Test is available in three versions to allow efficient testing of the various configurations of the Model III Computer. This allows the technician maximum flexibility in testing RAM, ROM, and Video Memory.

1. BURNINL/CMD — for cassette tape loading
2. BURNDOS/CMD — for Disk System Memory Tests
3. BURNINH/CMD — for testing low memory (requires 48K RAM)

Features

Test Dynamic Ram, Video Ram, and Rom in the Model III Computer.

Tests data retention under wait states (refresh suspended) by utilizing wait states and the "waitimout" circuit on the FDC card (in disk systems only).

Advantages

Allows the technician to verify all memory in the Model III computer. Shows a "day:hour:minute:second" format on the screen to aid in identifying time related problems. Checks ROMS and displays checksums on each pass of the test. Checks dynamic and video RAM by a random pattern method.

LOADING, EXECUTING BURNIN TEST

BURNIN/CMD:

<<< THIS VERSION WILL NOT RUN OR LOAD WITH TRSDOS!! >>>

This version is supplied on diskette. IT IS NECESSARY TO TRANSFER THIS VERSION TO TAPE BEFORE USING! Use the TRSDOS "TAPE" command to transfer to cassette:

Connect the cassette recorder to Model III and set it to the RECORD mode with a blank cassette installed. Make sure the cassette is advanced past the leader.

In TRSDOS command mode type "TAPE (S=D,D=T) <ENTER>".

TRSDOS will prompt "CASS?".
Reply "H" for 15ØØ BAUD

TRSDOS will prompt "DEVICE = DEVICE TO TAPE - FILESPEC?"
Reply "BURNINL/CMD <ENTER>"

"PRESS ANY KEY WHEN READY" will be displayed. Do so, and tape version will be written.

To load and execute the tape version, enter BASIC (non-disk), prepare cassette, and type:
"SYSTEM <ENTER>"

At the "*?" prompt reply "BURNINL <ENTER>"
At program will now load from cassette.

At the "*?" prompt reply "/ <ENTER>" to execute program.

BURNINH/CMD, BURNDOS/CMD:

In TRSDOS command mode type:

"BURNINH/CMD <ENTER>" to execute BURNINH
"BURNDOS/CMD <ENTER>" to execute BURNDOS

DESCRIPTION OF TEST

The programs initially prompts for System Memory Size:
(1)=16K (2)=32K (3)=48K.
Type 1 to test a 16K machine, 2 for a 32K machine, and 3 for a 48K machine.

ROM TEST:

Upon entering the Memory Size, the program begins with a ROM checksum test (accumulates an additive total of ROM data bytes). The ROM checksum is displayed on the top line of the video display in the following manner:

ROM A	ROM B	ROM C
BBC4 DA75	4Ø7C	2EF8

The first two 4 digit hexadecimal numbers from the left (BBC4 DA75) represent the checksum of the first ROM A (U1Ø4). The next 4 digit hex number represents the checksum of ROM B (U1Ø5). The next 4 digit hex number represents ROM C (U1Ø6).

Current Valid ROM Checksums

ROM A		BBC4 DA75
ROM B		4Ø7C
ROM C	early mfg. no 8ØØ4Ø316	2B91
	no production REV A	278A
	mfg. no. 8Ø4Ø316 REV B	2EF8
	mfg. no. 8Ø4Ø316 REV C	2F84
	Network III	2764
	Network III	276A

**** NOTE ****

ROMS with slow access times may not be found faulty by this method of testing.

VIDEO/DYNAMIC RAM TEST:

The memory test is accomplished as follows:

First a random number is generated. This number is used as a starting point for testing. The memory under test is filled with an incrementing pattern from this random starting point. After the memory is filled with this test pattern, the program compares each memory location to see if the data written to that location is still stored there.

The random number is then rotated left once and the memory filled and compared again. This rotation takes place eight times and then another random starting number is generated.

When a dynamic RAM error is found, the video screen will show the location of the faulty IC in split hex format (High side and low side) and by IC location on the logic board (i.e. "U48").

If a fault is found in video RAM the fault message may appear altered as a function of the failure. In this case compare the ASCII code you see with the correct code to determine which bits are incorrect.

BURNINL/CMD

BURNINL/CMD resides from 43ØØ hex to 4B33H. This version is incompatible with TRSDOS, and can only be loaded and executed from tape. This version does not test the memory for data retention with WAIT states as the other versions do, since that feature requires an FDC to be present in the machine.

BURNDOS/CMD

The "BURNDOS/CMD" program resides from 52ØØH to 5A33H. If low memory (4ØØØH to 5A33H) is good then the program can be loaded from disk to find a faulty RAM in high memory. The test is basically the same as "BURNINL/CMD" except that the program will test the 2 millisecond dynamic RAM refresh specification by using the "waitimout" ring counter on the FDC board. This is accomplished by selecting the motor on signal to generate two 1 millisecond delays thus forcing the CPU into a 2 millisecond waitstate. The drive motors will run for the first six minutes of each hour the test is run.

BURNINH/CMD

This program allows testing of low memory as it resides from F82AH to FFFFH. This requires that the computer to be tested contain 48K of memory. The program is basically identical to "BURNINL/CMD" except that it is located in high memory. If the machine to be tested does not contain 48K of RAM then the technician must install "known good" RAM in order to execute this program.

Troubleshooting Hints:

Difficult to locate or heat related problems may take several passes. To help detect heat related problems, hot or cold air may be applied during the tests.

It may require several hours to locate a fault affecting only one memory bit.

A binary sequence will test RAMS in the "low bit" positions more than in the "high bit" positions. Due to this property, it may be advantageous to exchange the RAMS in the "high side" positions (D4-D7) with those in the "low side" positions (DØ-D3), if a memory problem is suspected but not found in a reasonable period of time.

Random faulty bits or multiple chip failures may be an indication that the decoders, multiplexers, or buffers are causing problems.

The RAM banks should be visually examined to determine that all pins on all chips are in place and that the memory jumpers are in the correct positions. A check of +5, +12, and -5 volt power should also be made at that time.

NOTE: RAMS with improper voltages applied (i.e., - the five volt pin not inserted correctly) have been known to pass this test.

No one memory test is totally conclusive; therefore, use all the memory tests available in difficult situations.

MEM6

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MEM6

General Description

The MEM6 memory diagnostic program provides the computer technician with a method of checking all areas of Model III memory: RAM, ROM and Video RAM.

Features

Three different algorithms for RAM testing, including:
- Quick Test
- Push-Pop Test
- Complete Test

ROM testing by checksum
Video RAM testing includes display of all character and graphics set.
Menu driven.

LOADING AND EXECUTING MEM6

Disk systems:

Disk version: Boot TRSDOS, insert the disk containing MEM6/CMD and type: MEM6 <ENTER>

Tape version: First, transfer MEM6 to disk, as described later. Then, load and execute the disk version.

NOTE: The tape version will NOT load directly into RAM under either Disk Basic "System" or the Tape utility due to memory usage conflicts.

Cassette systems:

Apply power. The system will prompt: Cass?
Respond with "H"

The computer will then prompt: Memory Size?
Press <ENTER>

Upon receiving the "READY" message, type: SYSTEM <ENTER>

The computer will prompt: *?

Ready cassette, then type: MEM6 <ENTER>

When the cassette has finished loading, the systems prompt will return. Type a slash and then press <ENTER>

You are now ready to choose the desired test.

TEST DESCRIPTIONS

ROM TEST

The ROM test is performed by the computer adding up the hexadecimal value of all the bytes in each ROM. The total for each ROM is then displayed on the screen, along with what the total should be. If the checksums match, the ROM is assumed to be good. This assumption is reasonable because it would take offsetting errors of equal amplitude to indicate the correct checksum falsely and the odds against that occurrence are tremendous.

One special cause that exists is the fact that the addresses for ROM C include the printer status port. This would normally cause the checksum to vary according to whether or not a printer was connected; online, busy, out of paper, or whatever. In order to compensate for this, after the computation of the checksum for ROM C, the values of the bytes at 37E8H and 37E9H are subtracted from the total. Thus the status can only affect the checksum if it changes at exactly the right moment in the program, which is difficult to do.

To execute the ROM test, simply type "0" when the program prompts you for the desired test.

RAM TEST

When the main menu prompts "Which Test?" typing an "A" will cause the program to enter the RAM test mode. The operator will then be prompted for which one of the RAM tests desired.

Quick Test ("Q")

The Quick Test should be run first, as it will detect any "hard struck" bits. The test first computes the end of memory and then insures that each byte location in the available range can be cleared (set to ØØ) and set to FF. This is indeed quick and will certainly point out obvious hard errors such as those caused by missing a pin while plugging the Ram chip into the socket.

Complete Test ("C")

The Complete Test is similar to the Quick Test in that all memory locations are tested for the ability to store and retain a specific variable. It differs from the Quick Test in that each location is tested for the ability to store each of the 256 possible bytes with adjacent locations containing different bytes. Consequently this test takes quite a bit more time to execute than the Quick Test.

Push-Pop Test ("P")

The Push-Pop Test differs from the other two RAM tests in that it has no logical end. It is therefore useful as a long-term test to locate intermittent or otherwise hard to locate memory problems. This test uses the stack pointer to push a variable into memory and later pop the variable to see if the memory retained the correct value.

VIDEO TEST ("V")

MEM6 provides a method of not only checking the video RAM, but displaying all the characters available on the Model III. Each video RAM location is tested for the ability to store each of the possible data combinations and its corresponding character representation is displayed on the screen. The data is shifted sequentially through the RAM addresses rather rapidly. To stop the display at any point press the "H" key. For a more detailed description of this and other information, see the section entitled "Keyboard Interaction".

Should MEM6 detect a video RAM error while in the VIDTEST mode, it will immediately report the chip it finds to be bad, and then stop execution. This is different from the regular RAM test, which continues execution and reports additional errors encountered. The reason for this is due to the algorithm used to report the video error. Therefore, any time a video chip is reported to be bad, that chip should be replaced and the program run again. Since there are only two video RAM chips, this will not be a time consuming venture. One final note, it should be stressed that if the video RAM is bad, the chip that it reports as bad might be a wrong number or even a letter or other character, if the video RAM is bad in the location where the number of the bad chip is to be displayed.

ERROR REPORTING -- ALL RAM TESTS

MEM6 is designed to report any RAM chip it determines to be defective by row number and "V" number. Note that if many RAM chips are reported to be bad and replacing them does not correct the problem, then the actual defect could be a memory related component such as an address buffer, a data buffer, or a multiplexer. It is also important to note that memory occupied by the program itself is not tested. In case of bad memory in the location the program would not load or execute correctly. In the case of a disk system with problem RAM in this area, one might not be able to boot. If trouble is suspected in this area, the best procedure would be to put known good RAM in the first 16K (upper sockets) and move the suspect chips to another location for testing.

All RAM tests except the Push-Pop Test will report their completion. If completion is reported without any reported failures then the RAM is assumed to be good.

KEYBOARD CONTROL

The operator has a limited amount of intervention during program execution of MEM6. There are two different times when the operator can intervene: while in the main menu and during actual execution of one of the modules. It should be noted that during the actual execution of the module, the keyboard is only polled immediately following the printing of a character on the screen. Therefore, during execution of a module, a key must be held down until the next character is printed.

MAIN MENU

In addition to the commands ("O", "A", and "V") which are available while in the main menu, there is an "X" command. Entering an "X" from the main menu will cause the system to reboot if it is a disk system, or to go back to the "Cass?" prompt if it is a cassette system. In other words, the "X" command is the same as pressing the reset button, except that there is no danger of losing refresh as there is with pressing the reset button.

MODULE INTERVENTION

The following keys will be effective during module execution, subject to the restrictions mentioned above in the section entitled KEYBORAD CONTROL.

"H" - Halts the execution of the module and waits for entry of one of the two following commands:

"C" - Continues execution of the module. To be used only after the "H" command.

"E" - Exits the module and returns to the main menu. Valid any time.

TRANSFERRING MEM6 TO DISK

Prepare the MEM6 tape and use the TRSDOS "Tape command:

Boot TRSDOS and type: TAPE (S=T,D=D) <ENTER>
The program will prompt: Cass?
Respond with "H"

When the program is completed, MEM6/CMD will be listed in the drive directory.

DT-1 DIAGNOSTICS
DT1DIAG

CHAPTER 4

TABLE OF CONTENTS

DATA TERMINAL-1 TEST

General description

The Data Terminal-1 Test programs (DT1DIAG's) are designed to aid in the detection of certain visual-attribute problems, which may otherwise become non-perceptive to the user. The data, being sent to the DT-1 via RS-232C, inputs various codes which command the 8Ø51 (CPU) to execute distinct, internally programmed schemes that control many of the visible and non-visible display features of the terminal. Since DT1DIAG is executed by a host computer and all program entries are made on the DT-1, the program is actually testing the receive circuitry of the DT-1, along with output data from the terminal. If the DT-1 transmits and receives properly, the program should execute effectively.

Features

Self-prompting user oriented software
Selectable execution speed (Baud = 75 thru 19200)
Fast memory fault detection
Allows the video memory to be tested
Allows internal (CPU) program memory to be tested
Provides a positive affirmation of properly functioning video circuitry
Fast access to Self-Test *(special DT-1 trace feature)

DATA TERMINAL-1 OPERATION

First, insure that you have the proper cable interfacing the DT-1 and the Model III. A Null Modem adapter (26-1496) must be used along with the (26-14Ø8), or similar RS232 cable. Connect one to the Model III, RS232 (DB25) on the bottom side of the Model III, and the other end to the Null Modem Adapter. The other end of the Null Modem adapter should connect to the inner-most DB25 (HOST) connector of the DTl, bottom side.

You should next view the 'SET UP' configuration of the DT-1 as shown in this manual, Appendix A. To do this type:

<CTRL/SHIFT/ENTER> simultaneously on the DT-1

To change any of the options, simply type in a <1> or a <Ø> at the proper location after moving the cursor with the arrows on the keypad. Once the 'SET UP' is in order, as on page 2, type <ENTER>.

The DT-1 will ask if you want to store permanently.
Type <N>

Now type <SHIFT/BREAK> together. A Bell will sound and a blinking-block cursor will appear at home position. The DT-1 in now ready. If trouble should arise while performing this, refer to the 'SET UP' instructions of the DT-1 owners' manual.

SETTING UP THE MODEL III

After booting in TRSDOS 1.3, type <DTHOST> on the Model III. This is a special Host program to allow you a faster and easier method of intializing serial communications between the DT1 and the Model III. After DTHOST has been loaded it will prompt you with its default parameters as follows:

BAUD = 96ØØ, WORD = 8, STOP = 1, PARITY = ODD, NO WAIT MODE

To change any of these, type a <SHIFT><DOWN ARROW><S> simultaneously on the Model III. The cursor will move to home position. Now type as follows:

B=12ØØ <ENTER> To change baud rate.
or
S=2 <ENTER> To change to 2 stop bits.

A complete Model III SETCOM HELP is listed in Appendix B. The same help listing is also contained within the DT1DIAG program and is accessed by typing a <98> from the Menu prompt.

*** NOTE *** The BREAK key on the DT-1 will temporarily pause the video on the DT-1; it will NOT break a TRSDOS execution, but a <CTRL/C> when typed on the DT-1 will break TRSDOS execution.

MODEL III LOADING and EXECUTING DT1DIAG

After you are sure that BOTH the DT1 and the Model III are set to the same RS232 parameters, type:

<BASIC DT1DIAG> <ENTER>

Do this on the DT1 or the Model III. There is no need to enter any more data from the Model III, since communications are already in progress.

From this point on ALL entries to the program should be made on the DT-1 to insure proper serial data transmission from the DT-1 to the Host. Be sure the <CAPS LOCK> key has been depressed.

The ONLY exception to this is when changing the Model III's RS232 parameters, the <shift><down arrow><S> must be typed on the Model III.

To change the DT1 parameters, refer back to the SET UP mode.

DT-1 DISPLAY FORMAT

The following should be displayed on the DT-1. If it is NOT then try lowering the BAUD rates of both the Model III and the DT-1. Refer to Model III 'Setcom' instructions and the DT-1 'SETUP' instructions in the appendicies attached.

DATA TERMINAL 1 TEST

The test is self-prompting with menu features. It will print a display, then prompt the Mode in which it printed along with their instructions.

Hit <ENTER> to continue ?

After typing <ENTER> the following menu will be displayed in reverse video. If there is NO reverse video (a white screen) a possible problem may be present with U25, an EEPROM. If the display has double ASCII characters, go back to the 'SET UP' and insure that the F/H (full duplex) is <Ø>.

MODEL III/DT1 MENU DISPLAY

```
BAUD = 96ØØ  WORD = 8  STOP = 1  PARITY = ODD  NO WAIT MODE
-----------------------------------------------------------

1     NORMAL                          2     INVISIBLE
3     BLINK                           4     INVISIBLE
5     REVERSE                         6     INV BLINK
7     REV BLINK                       8     REV INV BLINK
9     UNDERLINE                       1Ø    INV UNDERLINE
11    BLINK UNDERLINE                 12    INV BLINK UNDERLINE
13    REV UNDERLINE                   14    INV REV UNDERLINE
15    REV BLINK UNDERLINE             16    INV REV BLINK UNDERLINE
17    1/2 INTENSITY TEST              18    CURSOR ON/OFF TOGGLE
19    TURN ON DT1  **  MONITOR  ** FEATURE

77    RUN COMPLETE TEST
98    MODEL III SETCOM HELP
99    EXIT DT1 TEST?
```

Simply enter the <##> of the test you wish to perform and DT1DIAG will prompt you with any further instructons.

(example) <3> <ENTER>

** NOTE ** The prompt at the bottom of the screen:

'HIT <ENTER> to check if BLINK video is OK ?'

```
**********************************************************
*      ***THE SCREEN SHOULD IMMEDIATELY RETURN ***    *
*           to a NORMAL video after <ENTER>           *
**********************************************************
```

MODULE DESCRIPTION

<1> Will fill screen with the word 'NORMAL'

<2> The cursor will move across the screen printing non-visibly the word 'INVISIBLE'. To insure the video suppression output of the 8276 CRTC (U7) is functional, perform this test. Again, hit <ENTER> to check if 'INVISIBLE' was indeed placed into the 2114's (video RAMS).

<3> Video should be filled with the word 'BLINK' and also should be blinking. This is caused by the General Purpose output of U7 to U2 latching dot information of U9.

<4> Same as menu item 2, but a different code was issued.

<5> The word 'REVERSE' repeated in Black-On-White is caused by U1Ø and U3 logic, originated white by U7 and the black printing caused by BOW from U12.

<6> A plain white video screen. ASCII was suppressed by signal VSP of U7 and its associated logic.

<7> A white screen with ASCII blinking on/off.

<8> ASCII blanked, white screen.

<9> Video is normal with UNDERLINE underlined.

<1Ø> Underlining performed with suppressed ASCII.

<11> ASCII written to normal video with underlining.

<12> Underlining is blinking with no visible ASCII.

<13> A white screen with ASCII and underlining.

<14> A white screen with NO ASCII but with underlines.

<15> A white screen with both ASCII and the underlines blinking.

<16> A white raster with blinking underlines but no visible ASCII, until <ENTER> is depressed.

<17> This is a test of changing the amplitude of the video signal, therefore allowing a grey/white or a dimmed ASCII display. This is caused by adding a portion of a logic Ø at the time of video dot output. If no apparent difference, check U11 U1.

<18> Toggles the cursor OFF or ON.

<19> **At this entry, the DT-1 will NOT perform any of its unique attributes, but will rather inform you of EVERY code it received through RS232 from the HOST. Use this test to check internal ROM programming of the 8Ø51 CPU in case some of the previous tests worked and some did not. Check the codes received against the codes in the owners manual.
(displayed) <EcG4> should turn Reverse video on. If you did receive the proper codes and they were not performed correctly then either the 8Ø51 or U25 or associated circuitry should be suspected at fault.

MEMORY MAP DECODING for DT1

External to the CPU's memory (4Kx8 ROM) is a total of 2K RAM (4x 2114's) used for Video RAM, a EEPROM (X2210 nonvolatile) which are all only accessable by the CPU for reads or writes. These memory locations are memory mapped. Address decoding is accomplished by U16 (a 1 of 8 decoder). Address lines A10 thru A13 are monitored by U16.

NOTE: The line A13 must be high while addressing any memory external to the CPU. Decoding is segmented into 1K byte pages.

A13	A12	A11	A10	DECODED MEMORY SUBSECTIONS
1	0	0	0	Low Video memory U26 and U28
1	0	0	1	High Video memory U27 and U29
1	0	1	0	Non-volatile memory X2210l U25
1	0	1	1	Keyboard Read select to U6
1	1	0	0	Keyboard RS232C input Read U23
1	1	0	1	Non-volatile RAM WRITE select (U11)
1	1	1	0	NOT USED
1	1	1	1	CRT (8276) controller select

APPENDIX A

DATA TERMINAL 1 TEST

SET UP

TC1	TCØ	EM1	EMØ	REV	DTR	DSR	DCD
Ø	Ø	Ø	Ø	Ø	1	1	1

STB	O/E	PAR	WDL	BR3	BR2	BR1	BRØ
Ø	Ø	Ø	Ø	1	1	1	1

ALF	AWP	F/H	CT1	CTØ
Ø	1	Ø	Ø	Ø

MNEMONIC		DESCRIPTION OF TABLE
TC1	TCØ	Selects TERMINATING CHARACTER
Ø	Ø	CARRIAGE RETURN
Ø	1	CARRIAGE RETURN/LINE FEED
1	Ø	END OF TEST
1	1	END OF TRANSMISSION
EM1	EMØ	Selects EMULATION MODE
Ø	Ø	TELEVIDEO 91Ø
Ø	1	LEAR SIEGLER ADM-5
1	Ø	ADDS 25
1	1	HAZELTINE 141Ø

REV	REVERSE VIDEO	(IF SET TO <1>)
DTR	DATA TERMINAL READY	(<1> = CONNECTED)
DSR	DATA SET READY	(<1> = CONNECTED)
DCD	DATA CARRIER DETECT	(<1> = CONNECTED)
STB	STOP BITS	(Ø=1 bit 1=2 bits)
O/E	ODD or EVEN PARITY	(Ø=odd 1=even)
PAR	PARITY SELECT	(<1> = SELECTED)
WDL	WORD LENGTH	(Ø=8 bit 1=7 bit)

BR3	BR2	BR1	BRØ	Selects BAUD rate of RS232 I/O
Ø	Ø	Ø	Ø	96ØØ
Ø	Ø	Ø	1	75
Ø	Ø	1	Ø	11Ø
Ø	Ø	1	1	15Ø
Ø	1	Ø	Ø	3ØØ
Ø	1	Ø	1	6ØØ
Ø	1	1	Ø	12ØØ
Ø	1	1	1	24ØØ
1	Ø	Ø	Ø	48ØØ
1	Ø	Ø	1	96ØØ
1	Ø	1	Ø	192ØØ (HIGHER COUNT DEFAULTS TO 96ØØ)

ALF	AUTOMATIC LINE FEED <1>	
AWP	AUTOMATIC WRAP <1>	
F/H	FULL DUPLEX (Ø)	HALF DUPLEX (1)

CT1	CTØ	Select CURSOR type
Ø	Ø	Blinking block
Ø	1	Blinking underline
1	Ø	Steady block
1	1	Steady underline

APPENDIX B

Model III DTHOST HELP:

BAUD = 96ØØ WORD = 8 STOP = 1 PARITY = ODD NO WAIT MODE

To Change Model III RS232 parameters, at any prompt press:

<shift><down arrow><s>

on the Model III, then type the desired parameters:

<ENTER> to display current setup
() <ENTER> to set to the default parameters.

(B=n1, W=n2, S=n3, P=n4, wait switch)

n1=baud rate: 5Ø/75/11Ø/134/15Ø/3ØØ/6ØØ/12ØØ/18ØØ/2ØØØ
24ØØ/48ØØ/72ØØ/96ØØ/192ØØ

n2=word length: 5/6/7/8

n3=stop bits: 1/2

n4=parity: 1=odd, 2=even, 3=none.

** DTHOST does NOT allow you to use the WAIT mode **

ex.- (B=24ØØ,W=7,S=2,P=3,NO)

Any parameter may be entered by itself: ex.- (B=24ØØ)
Once values are entered, type <ENTER> to continue the program

APPENDIX C

DT-1 CABLE INTERFACING

DT-1 (DB25) PIN ##		Host computer (DB25) PIN ##
1 PGND	----------	1 PGND
2 TD	----------	3 RD
3 RD	----------	2 TD
4 RTS	----------	5 CTS
5 CTS	----------	4 RTS
6 DSR	----------	8 CD
6 to 2Ø	-- tie DSR to DTR --	6 to 2Ø
7 SGND	----------	7 SGND
8 CD	----------	6 DSR

** NOTE ** The (26-1496) Null Modem adapter eliminates any need of rewiring RS232 cables or connectors. Use it whenever connecting a DT1 directly to a Host computer.

APPENDIX D

```
100 '            **********************************
110 '            *         DT1 DIAGNOSTIC         *
120 '            *  for Model III TRSDOS 1.3      *
130 '            *      March 15, 1982            *
140 '            **********************************
150 CLS:CLEAR (1500):DIMV$(30):DEFUSR0=&HF0DB:X=USR(0)
160 '           ***     INITIALIZE DT1 CODES     ***
170 B$=CHR$(7):PRINT"BELL !!";B$
180 CL$=CHR$(27)+CHR$(42):'CLEAR SCREEN (w/NULLS)
190 RV$=CHR$(27)+CHR$(71)+CHR$(52):'REVERSE VIDEO
200 MT$=CHR$(27)+CHR$(85):MONITOR ON
210 CI$=CHR$(27)+CHR$(46):'CURSOR INVISIBLE
220 NV$=CHR$(27)=CHR$(71)=CHR$(48):'NORMALVIDEO
230 HC$=CHR$(30):'HOME CURSOR
240 ST$=CHR$(27)+CHR$(86):'SELF TEST
250 HI$=CHR$(27)+CHR$(29):'1/2 INTENSITY ON
260 IO$=CHR$(27)+CHR$(28):'1/2 INTENSITY OFF
270 BL$=CHR$(27)+CHR$(71)+CHR$(54):'REVERSE BLINK VIDEO
280 F=0:'Set 'F' flag null for 1st run
320 PRINTCL$:FORI=1TO16:READV$:V$(I)=V$:NEXT
330 W=0:IFF=1THENJ=48:T=J-47:GOTO450
340 PRINT:PRINT:PRINTCL$;:PRINTRV$:PRINTSTRING$(24,"=");"   DT1   TEST
    "STRING$(24,"="):PRINT:PRINT:FORM=1TO15STEP2:PRINTM"      ";V$(M),M+1;"
    ";V$(M+1):NEXTM:T=0
350 PRINT" 17      1/2 INTENSITY TEST"," 18     CURSOR ON/OFF TOGGLE"
360 PRINT" 19       TURN ON DT1    **MONITOR**  FEATURE":PRINT:PRINT"
    77", "RUN COMPLETE TEST"
370 PRINT" 98","MODEL III SETCOM HELP":PRINT" 99","EXIT DT1 TEST";
380 INPUT:J=T+47:F=0:IFT=99THEN710
390 PRINT:PRINTNV$;CL$;:IFT<=0THEN340
400 IFT=19THENPRINTCL$:PRINTMT$:PRINT"*****TO     EXIT    THIS   MODE
    HIT   [SHIFT/BREAK]*****":T=0:PRINT"THEN [ENTER] ":GOTO340
410 IFT=77THENF=1:GOTO330
415 IFT=98GOTOSUB800:GOTO340
420 IFT=18THENPRINTCI$;:GOTO340
430 IFT=17THEN590
440 PRINTCL$;:PRINTCHR$(27)+CHR$(71)+CHR$(J);
460 M=1848/LEN(V$(T))
470 FORX=1TO M:PRINTV$(T);:NEXTX:IF J=48 THEN 490
480 PRINTNV$;:PRINT" Hit [ENTER] to check if ";V$(T); " vide ";
490 INPUT" OK ";Y:PRINTHC$;:PRINTV$;"     ";
500 FOR K=1 TO 500:NEXTK:PRINTCL$;B$;
510 INPUT"Type [R] for a repeat of this mode or {ENTER} to continue ";Y$
520 IFY$="R"THEN PRINCL$;:Y$="":GOTO450
530 IFF=1THENJ=J+1:T=T+1
```

```
54Ø INPUT"Type [T] for {SELF-TEST} or [ENTER] to continue ";Y$
55Ø IFY$="T"THENPRINTST$:FORB=1TO2ØØØ:NEXTB:PRINT"O";:Y$=""
56Ø IFF=1THENIFJ<64THEN45Ø  IFJ<64THEN45Ø
57Ø GOTO34Ø
58Ø PRINTCL$;:CLS:PRINT" BELL";B$FORB=1 TO 5ØØ:NEXTB:PRINTCL$:W=Ø
59Ø PRINTCHR$(27);")";"THIS IS 1/2 INTENSITY {ON} ":W=W+1
6ØØ PRINTCHR$(27);"(";"THIS IS 1/2 INTENSITY {OFF}"
61Ø PRINTRV$;:PRINTCHR$(8);:IFW=1THEN59Ø
62Ø PRINTNV$:W=Ø:INPUT"   Type  [R]  to   repeat   1/2  intensity  toggle
    ";Y$:IFY$="R"THENPRINT;:Y$=""GOTO59Ø
63Ø GOTO33Ø
64Ø PRINTCL$;:PRINTRV$;:PRINTBL$;
65Ø FOR E=1TO 83Ø:PRINT" ";:NEXTE:PRINT"DT1 TEST
    COMPLETE";:FORB=1TO3ØØØ:NEXTB:PRINT:PRINT:PRINT,NV$;
66Ø PRINT"[Q] to EXIT  test and [ENTER] to REPEAT entire DT1   test
    ";:PRINTBL$;:INPUT$;
67Ø IFY$="Q"THEN71Ø ELSERESTORE:GOTO33Ø
68Ø DATA"   NORMAL        ","    INVISIBLE","   BLINK       ","  INVISIBLE","
    REVERSE      ","   INV BLINK    ","  REV BLINK","  REV INV BLINK","
    UNDERLINE"
69Ø DATA"   INV  UNDERLINE","  BLINK UNDERLINE","  INV BLINK UNDERLINE","
    REV UNDERLINE"," INV REV UNDERLINE"," REV BLINK UNDERLINE"
7ØØ DATA" INV REV BLINK UNDERLINE"
71Ø PRINTCL$;CI$:PRINTRV$:FORX=1TO12:PRINTCHR$(1Ø);:NEXT
72Ø FORY=1TO32:PRINTCHR$(8);:NEXTY
73Ø BL$=CHR$(27)+CHR$(71)+CHR$(58)
74Ø FORP=1TO18:READK$:PRINTBL$;:PRINTCHR$(8);CHR$(8);CHR$(8);:NEXTP
75Ø PRINTCI$;CHR$(1Ø);"
76Ø FORT=1TO8ØØ:NEXTT
77Ø DATAE,T,E,L,P,M,O,C,  ,T,S,E,T,  ,1,-,T,D
78Ø PRINTCL$:CLS:END
8ØØ PRINTCL$:CLS
81Ø PRINT"To change Model III RS232 parameters, at any prompt"
82Ø PRINT"press <shift><down-arrow><s> on the Model III,"
83Ø PRINT"then type the desired parameters:":PRINT
84Ø PRINT"<ENTER> to display current setup"
85Ø PRINT"() <ENTER> to set to default parameters"
855 PRINT:INPUT"<ENTER> to continue";A$:PRINTCL$:CLS
86Ø PRINT"(B=n1,W=n2,S=n3,P=n4,wait switch)":PRINT
87Ø PRINT:n1=baud rate:5Ø/75/11Ø/134.5/15Ø/3ØØ/6ØØ/12ØØ/18ØØ/2ØØØ/
    24ØØ/":PRINTSTRING$(14," ");"48ØØ/72ØØ/96ØØ/192ØØ"
88Ø PRINT"n2=word length: 5/6/7/8"
89Ø PRINT"n3=stop bits: 1/2"
9ØØ PRINT"n4=parity: 1=odd,2=even,3=none"
91Ø PRINT"wait switch=wait for xmit char: NO=nowait,W=wait"
92Ø PRINT:PRINT"ex.- (B=24ØØ,W=7,S=2,P=3,NO)"
93Ø PRINT"any parameter may be entered by itself; ex.-(B=12ØØ)"
935 PRINT"Once values are entered, type <ENTER> to continue program."
94Ø PRINT:INPUT"<ENTER> to continue";A$:RETURN
```

I/O PORT TESTER

CHAPTER 5

Table of Contents

Model III & 4 I/O Port Tester

Introduction:

This is to acquaint you with the use of the Model III/4 I/O Port Tester, a device quite useful in troubleshooting the parallel I/O port on a Model III/4. It will help in verifying the proper operation of the I/O port without the customer bringing in their hard disk or other external devices.

Set Up:

First, connect the ribbon cable provided with the tester to the 5Ø pin connector on the back of the tester with the cable dressed down. This is the plug on the left as you look at the tester from the back. Next, hook the cable into the I/O port on the computer with the cable dressed out to the rear. Connect the power pack provided to the tester. Power up the computer first, then turn on the tester. **This sequence is important to avoid false errors.** The two LED's on the port tester should be illuminated at this time. If this is the first time this tester is being used then proceed to the alignment section.

Executing IOTEST/CMD:

You should type in: IOTEST <ENTER>

You should initially see:

********** MODEL III I/O PORT TEST **********

VERSION 2.4
AUG. 3, 1983

****

PRESS ANY KEY TO CONTINUE

The next prompt after this will be:

DO YOU WANT TO TEST THE "RESET" SIGNAL ? (Y/N OR <ENTER>)

If you elect to use this portion of the test you will be required to use the <RESET> button. This will necessitate having to re-install the program. Resetting should turn off both of the LED's at this time because the "RESET" signal clears the D latches that power the LED's. The RESET TEST should always be done the first time a unit is checked.

The next prompt after the RESET TEST will be:

ENTER THE CONTROL PORT VALUE IN HEX (<ENTER> = CF HEX)

Use the default value for this test.

The menu should now appear:

MENU

(A) AUTO TEST MODE
(L) LOOP TEST MODE
(S) SINGLE TEST MODE
(P) CHANGE PORT VALUE
(Q) QUIT TO OPERATING SYSTEM

****

(1) ADDRESS & DATA SIGNAL TEST
(2) ADDRESS SIGNAL ONLY TEST
(3) FORCED INTERRUPT TEST
(4) "WAIT" SIGNAL TEST

SELECT TEST MODE ? (A/L/S/P/Q)

You must first select the Mode that is to be used, then test number desired. <BREAK> will get out of any test, and return to the menu.

Test Modes

(A) AUTO MODE: This test will automatically proceed to the ADDRESS & DATA SIGNAL TEST. If this test passes, then it will skip ADDRESS ONLY TEST and go the INTERRUPT and WAIT tests. If test (1) fails then the ADDRESS ONLY TEST becomes an option by the user to help trace the error.

(S) SINGLE TEST MODE: If this mode is selected then any test (1-4) will be executed once.

(L) LOOP TEST MODE: This test will continually loop through any selected test (1-4). LOOP TEST is quite useful when troubleshooting with an oscilloscope because all signals are repetitive. You can exit LOOP TEST by hitting <BREAK>.

(Q) QUIT TO OPERATING SYSTEM: Returns to TRSDOS.

Detailed Test Descriptions:

(1) ADDRESS & DATA SIGNAL TEST: This test exercises the AØ-A7, DØ-D7, OUT*, IN*, and EXITOSEL ports. In this test, data is written out and certain ports are avoided. Data is read back to test for any change. Errors are displayed on the screen. If the RESET test was not done previously, this test will fail the first time through. In AUTO or SINGLE modes only eight errors can be displayed. In LOOP the first eight are shown, then it waits for any key to be depressed to continue the test. All data written out in LOOP is only one bit set at a time.

(2) ADDRESS ONLY TEST: This test generates (OUT ØCFH) and (OUT Ø3ØH) signals to toggle the two LED's on and off. Test points and instructions are also displayed.

(3) INTERRUPT TEST: Data signal, (OUT ØCFH), is fed into EXTIOBUS* port which causes the interrupt. A software flag tests as to whether the interrupt servicing routine has ever been accessed, and displays the result.

(4) "WAIT" SIGNAL TEST: This test generates the prompt, PLEASE WAIT 3 SECONDS. The one shot signal is generated periodically and fed to the WAIT* line. The CPU is forced into a WAIT state during the one shot.

I/O PORT TESTER SERVICE SECTION

Alignment, Troubleshooting, and Theory

If this is the first time that this tester has ever been used, it will require some calibration. The one shot, which is used in the WAIT test will have to be set to 1 millisecond. Use your oscilloscope on Pin 4 of U11. The INTERRUPT or WAIT test set for LOOP mode will provide continuous pulses from the one shot. Adjust R8, the pot next to the Dip Switch, until a 1 millisecond pulse width is obtained. WAIT also checks if a 1 millisecond wait will cause RAM refresh problems, so if there are problems with the program getting lost while doing this adjustment, shorten the one shot duration and run the test again. Best results are obtained if the one shot is started out at less than 1 millisecond and then adjusted to 1 millisecond.

Portions of U12 and U14 are used to light the LED's. If the LED's do not go off when doing the RESET test, look at Pin 13 on U12 or Pin 1 on U14 and hit <RESET>. These pins should go low, resetting the latches and turning off the LED's.

U3 is a bi-directional data buffer, a low on Pin 11 permits data flow in, a high switches it to data out. This IC would be a good suspect if the tester doesn't respond to the computer.

U1 and U2 are 2114 RAM's used to temporarily store data while testing. U16 and 1/2 of S1 are used as decoders for "3x" data, U13 and the other half of S1 are decoders for the "Cx" data. RAM Enable is controlled by 1/2 of U15.

1/2 of U9 is a one shot used in the WAIT SIGNAL TEST. It is the adjustable one shot mentioned previously. 1/2 of U12 and an inverting buffer in U11 are also used in conjunction.

The 'CF' decoder consists of U1Ø, U7, and U5. The '3Ø' decoder is U5, U6, U7, and U1Ø. Refer to schematic for specific sections and pinouts used.

Port Analysis:

"xF" Each write to this port will generate a "wait". This will cause LED A to change states.

Bit Ø A "1" written to this bit will generate an interrupt.

Bit 1 Not Used.

Bit 2 A "1" written to this bit will generate a DRQ pulse.

Bit 3-7 Not Used.

"xØ" Each write to this port will cause LED B to change states.

Bit Ø Not Used.

Bit 1 A "1" written to this bit will enable the RAMS.

Bit 2 Not Used.

Bit 3 A "1" written to this bit will enable the DATA buffer.

Bit 3-7 Not Used.

This is a table of addresses that can be set by the Dip Switches.

	S1			
"xF"	1	2	3	4
ØF	on	on	on	on
1F	off	on	on	on
2F	on	off	on	on
3F	off	off	on	on
4F	on	on	off	on
5F	off	on	off	on
6F	on	off	off	on
7F	off	off	off	on
8F	on	on	on	off
9F	off	on	on	off
AF	on	off	on	off
BF	off	off	on	off
CF	on	on	off	off
DF	off	on	off	off
EF	on	off	off	off
FF	off	off	off	off

	S2			
"xØ"	5	6	7	8
ØØ	on	on	on	on
1Ø	off	on	on	on
2Ø	on	off	on	on
3Ø	off	off	on	on
4Ø	on	on	off	on
5Ø	off	on	off	on
6Ø	on	off	off	on
7Ø	off	off	off	on
8Ø	on	on	on	off
9Ø	off	on	on	off
AØ	on	off	on	off
BØ	off	off	on	off
CØ	on	on	off	off
DØ	off	on	off	off
EØ	on	off	off	off
FØ	off	off	off	off

Construction Notes:

S4 is a 14 pin socket in a 2Ø pin position, pin 1 matches pin 1.

R1Ø is connected from U11 pin 12 (at the feed thru) to +5 vdc (at 'C7').

W1 connects the (2) 8 pin holes on the PCB near J1 and J2. The holes are numbered in order and hole 1 is on the same end in each set. The holes are connected 1-1, 2-2, ..., 8-8.

W2 connects pin 1 of U8 (at the feed thru) to pin 2 of U4.

W3 connects pin 1 of U4 to pin 1Ø of U7.

J3 is the Model III test connector and J1 is the Model II test connector.

Testing:

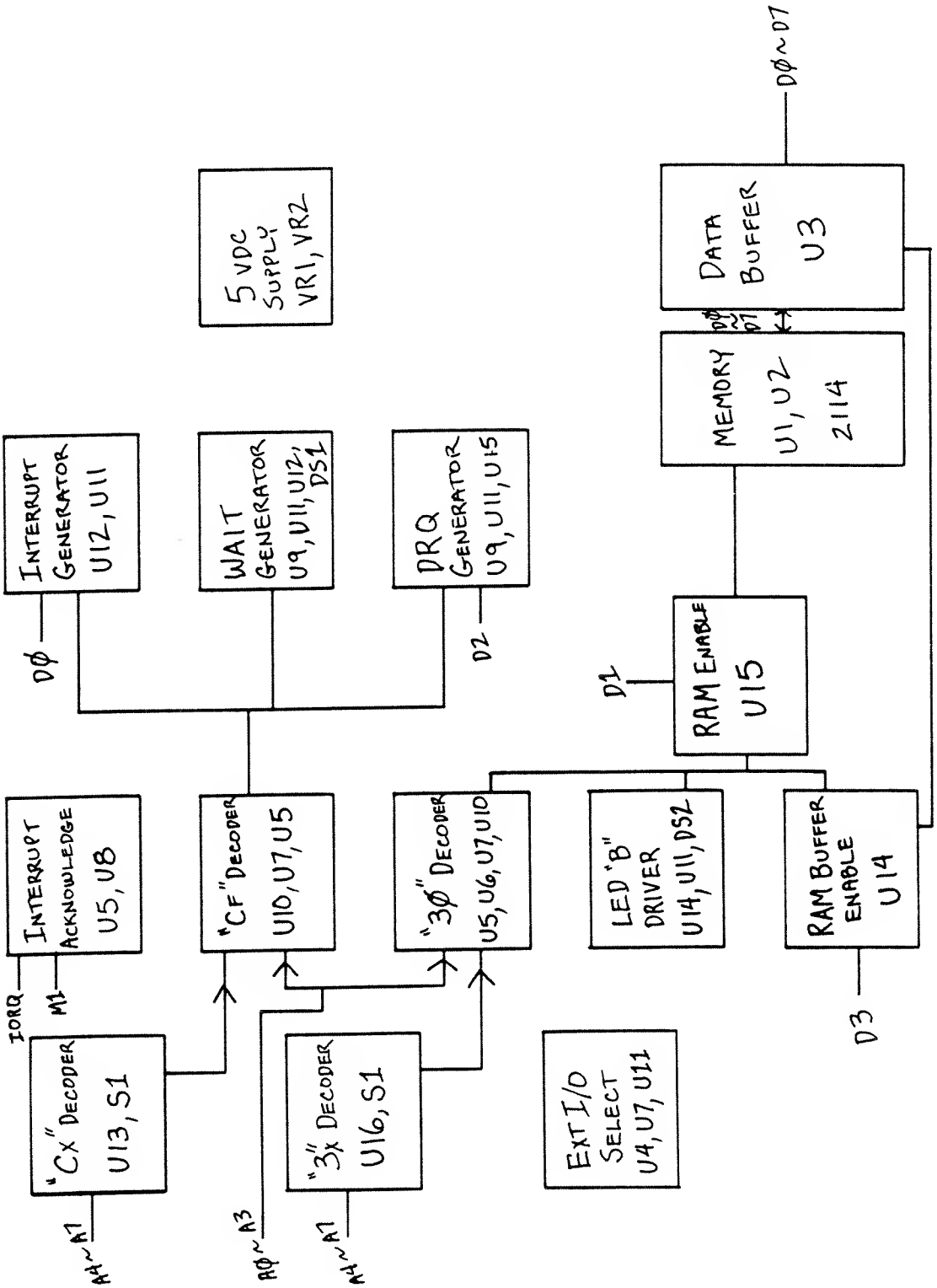
Set dip switch S1 to 1,2,7, & 8 on and 3,4,5,& 6 off. Turn R8 and R9 to the center position. The Power supply should be plugged into P1. The 5Ø pin cable should then be plugged into J2 on the I/O port tester and into the expansion bus on the Model III. The Model III and the I/O port tester are then turned on. The diagnostic disk should then be booted. Run the program 'IOTEST3'. Do not test reset, default the port address to CF, and proceed to the AUTO test. If the tester is functioning properly, all four tests should pass.

Troubleshooting Hints:

The Address & Data Signal Test is the most complete test of the I/O bus. If you get an error, execute the Address Only Test. This will isolate the errorto one of the two buses by checking the address but not the data bus. If no errors are found on this test then it would be a good guess that the data bus is the source of the errors on the A & D Signal Test. Use your oscilloscope to check for data (or lack of it) on the suspect bus.

In troubleshooting a failure on the interrupt test, it would be best to start at the I/O Port connector and step back through the interrupt circuitry using the oscilloscope to follow the signal. Use LOOP mode to get continuous interrupts.

Troubleshooting for failures on the WAIT Test should be done using the same techniques as on the interrupt test, check back through the wait circuitry to the Z-8Ø.



BLOCK DIAGRAM

I/O PORT TESTER PARTS LISTING

Parts list for the I/O port tester:

SYM	Name	Part No.
-	PC Board	17ØØ22Ø
Connectors		
P1	Connector 5-pin din	8519ØØ2
J1	Connector 5Ø-pin	8519117
J2	Connector 5Ø-pin	8519117
Wires		
W1	6" 8 cond wire	
W2	3" #3Ø KYNAR	
W3	3" #3Ø KYNAR	
W4	2' 5Ø cond cable	
Power Supply		
T1	Network III type power supply	879ØØØ2
Mechanical parts		
VR2	Heat sink, top	8549ØØ3
VR2	Heat sink, bottom	8549ØØ4
1Ø	Case, top	8719191
1Ø	Case, bottom	871919Ø
2Ø	Rubber foot, rear 1/4"	859Ø119
2Ø	Rubber foot, front 7/16"	8589ØØ5
6Ø	Screw 4x1/2 (PC Board)	8569151
4Ø	Screw #4x3/4 (case)	8569149
1Ø	Nut keep #4-4Ø	8579ØØ3
1Ø	Screw #4-4Ø X3/8"	8569ØØ2

Capacitors

C21	capacitor, .Ø1uf 5ØV 1Ø% mono	8383Ø4
C19	capacitor, .Ø2uf 1ØØV 2Ø% poly	8353225
C2Ø	capacitor, .Ø2uf 1ØØV 2Ø% poly	8353225
C1 through C16	capacitor, .1uf 5ØV mono rad.	8384Ø4
C18	capacitor, 22uf 16V elec. rad.	8326221
C17	capacitor, 47Øuf 36V elec. rad.	

Switches

S2	switch, PWR ON/OFF	8489Ø36
S1	switch, 16-pin dip spst	8489ØØ4

Resistors

R1	resistor, 22Ø ohm 1/4 W 5%	82Ø7122
R2	resistor, 22Ø ohm 1/4 W 5%	82Ø7122
R4	resistor, 47Ø ohm 1/4 W 5%	82Ø7147
R1Ø	resistor, 47Ø ohm 1/4 W 5%	82Ø7147
R3	resistor, 5.1k ohm 1/4 W 5%	82Ø7251
R7	resistor, 5.1k ohm 1/4 W 5%	82Ø7251
R6	resistor, 47k ohm 1/4 W 5%	82Ø7347
R5	resistor, 4.7k ohm 1/4 W 5%	82Ø7247
RP1	resistor, 4.7k ohm sip 8-pin	8292246
RP2	resistor, 4.7k ohm sip 8-pin	8292246

IC Sockets

S4	socket, 14- pin	85Ø9ØØ8
S5	socket, 14-pin	85Ø9ØØ8
S6	socket, 14-pin	85Ø9ØØ8
S7	socket, 14-pin	85Ø9ØØ8
S8	socket, 14-pin	85Ø9ØØ8
S1Ø	socket, 14-pin	85Ø9ØØ8
S11	socket, 14-pin	85Ø9ØØ8
S12	socket, 14-pin	85Ø9ØØ8
S14	socket, 14-pin	85Ø9ØØ8
S15	socket, 14-pin	85Ø9ØØ8
S9	socket, 16-pin	85Ø9ØØ3
S13	socket, 16-pin	85Ø9ØØ3
S16	socket, 16-pin	85Ø9ØØ3
S1	socket, 18-pin	85Ø9ØØ6
S2	socket, 18-pin	85Ø9ØØ6
S3	socket, 2Ø-pin	85Ø9ØØ9

IC's

U11	IC 7416 Hex inverter	8ØØØØ16
U13	IC 74S85 Comparator	9Ø1ØØ85
U16	IC 74S85 Comparator	9Ø1ØØ85
U6	IC 74LSØ4 Hex Inverter	8Ø2ØØØ4
U8	IC 74LSØ4 Hex Inverter	8Ø2ØØØ4
U7	IC 74LSØ8 Quad 2-in AND	8Ø2ØØØ8
U5	IC 74LS32 Quad 2-in OR	8Ø2Ø032
U12	IC 74LS74 Flip-Flop	8Ø2Ø074
U14	IC 74LS74 Flip-Flop	8Ø2Ø074
U15	IC 74LS74 Flip-Flop	8Ø2Ø074
U4	IC 74LSØ2 Nor Gate	8Ø2ØØØ2
U9	IC 74LS123 Multivibrator	8Ø2Ø123
U3	IC AM83Ø3 BUS tranceiver	8Ø6Ø3Ø3
VR2	Voltage Regulator 78Ø5 1.5A	8Ø5Ø8Ø5
U1	RAM 2114	8Ø42114
U2	RAM 2114	8Ø42114
VR1	Bridge rectifier VM28	

Leds

DS1	LED, red assy.	8469Ø12
DS2	LED, red assy.	8469Ø12

SCHEMATIC DIAGRAMS

REVISION				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

CONN. JUMPER 50 J2 *

PART OF J1 — PART OF J2

J1	J2	
32	49	IORQ*
	47	M1*
32	37	RESET*
46	NC	HDBWPOS (C8H)
20	17	A0
22	19	A1
24	21	A2
26	23	A3
25		A4
27		A5
29		A6
31		A7
34	NC	HDBCS* (C8-CFH)
28	33	RD*
43		EXTIOSEL
30	35	WR*
	45	HDBDRQ*
	39	IOBUSINT*
	41	WAIT*
	40	HDBINTRQ*
	42	HDBWAIT*
	50	EXCEPT PIN 50

U4 '02 — TO U7 PIN 9 IORQ

U5 '32 — U8 '04 — RESET2*, RESET*

U6 '04 — WR*, OUT

U7 '08 — OUTCF, OUT30

U10 '21 — 'XF', 'CX', 'XO'

U11 7416 — WAIT*, HDBDRQ*, IOBUSINT*

U12 '74 — DOE

U13 S85 — A=B OUT, A=B IN — DZE

U14 '74 — RESET* — DS2 — C21 .01UF

U15 '74 — RESET2* — D3E

U16 S85 — A=B OUT, A=B IN — D1E

RP1 4.7K — RP2 4.7K — "3H" — "CH"

R1 220 — DS1 — +5V

R2 220 — DS2 — LOCATED NEXT TO SWITCH

R3 * R8 5.1K 250K — 1MS — C19 .02UF

R4 470 — R5 4.7K — R6 47K — R7 5.1K — R9 100K — 300US — C20 .02UF

U9 '123 — CEXT C/R — A

INSEL* U3 PIN 9 — IORQ (FROM U4 PIN 13) — IN — N.C. — +5VDC VIA 720

PWR IN 5 PIN DIN — PWR SW — P1 — S2 — VM 18 — VR1

HEAT SINK — 7805C VR2 — C17 470 35V — C18 22 UF — 8-9VDC AVG I — 4.75 - 5.25 VDC — +5V — GND

DECOUPLING ONE .01UF CAP PER IC

ZEA '04 '04 '08 '16 '21 '32 '74 '74 '74 '85 '123 2114 8303 '02

.1 UF

U1, U2 2114 — A0-A7 — D7*-D0*

U3 AM8303 B:T/R — D7E-D0E

*NOTE: ALTERNATE SUBSTITUTION R3: 100K P.POT, R8: 100K POT. FOR 150K Ω NOMINAL = 1MS

NOTE: J2 PIN 50 IS ISOLATED FROM GROUND ON THE PCB & CONNECTS TO GROUND THROUGH J2 PLUG TO GROUND.

REF: DRILL PLAN 1700220

MATERIAL	UNLESS OTHERWISE SPECIFIED	NEXT ASSY	USED ON
FINISH	TOLERANCES XX=±.010 XXX=±.005 ANGLES=±1° HOLE DIA TOLERANCES .014-.250 = +.005 -.001; .251-.750 = +.008 -.001; .751-UP = +.015 -.001		
	DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING		
	DO NOT SCALE THIS DRAWING		

DRAFT		DATE
CHECK		DATE
DESIGN	K. STEELE	DATE 11/1/82
APPD Rev A	K. STEELE	DATE 12/14/82
APPD		DATE

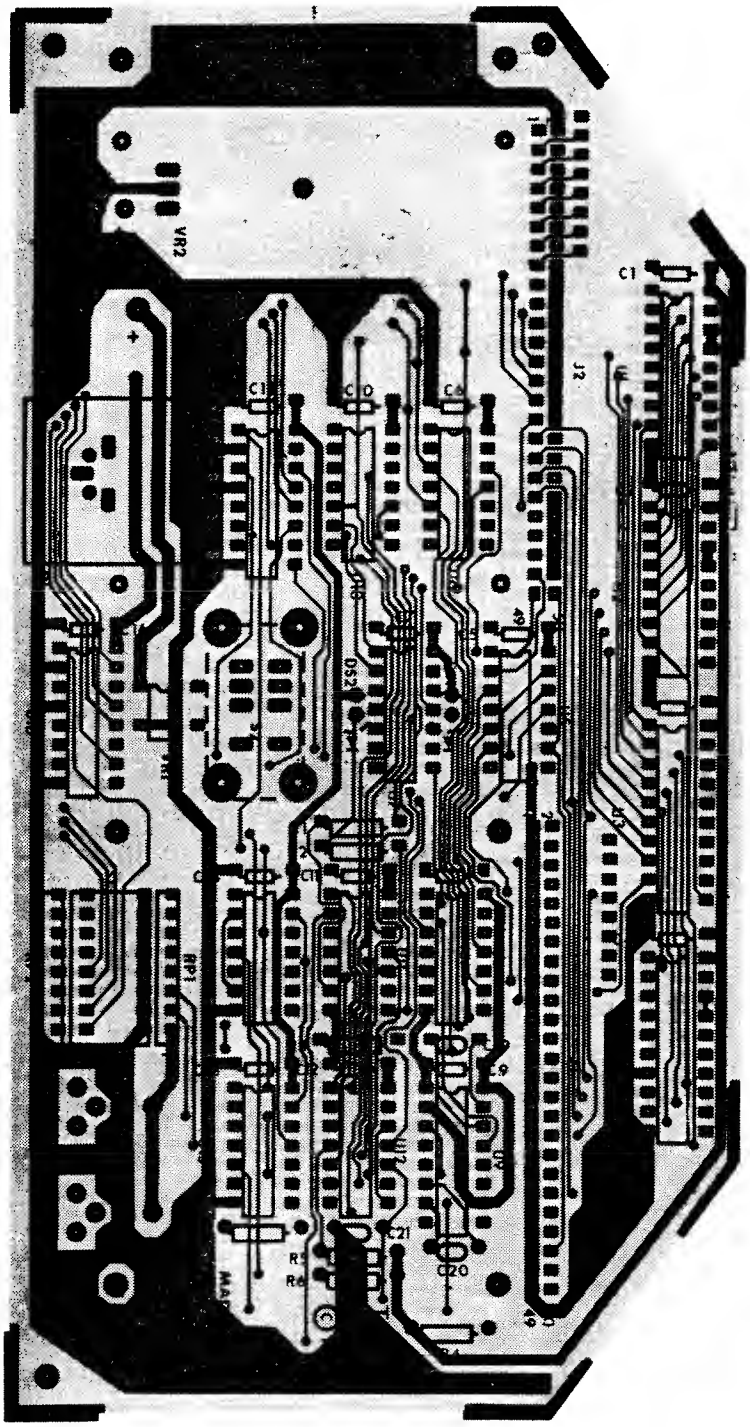
TITLE: MOD III, IV & MOD II/16 I/O PORT TESTER

6-13-83

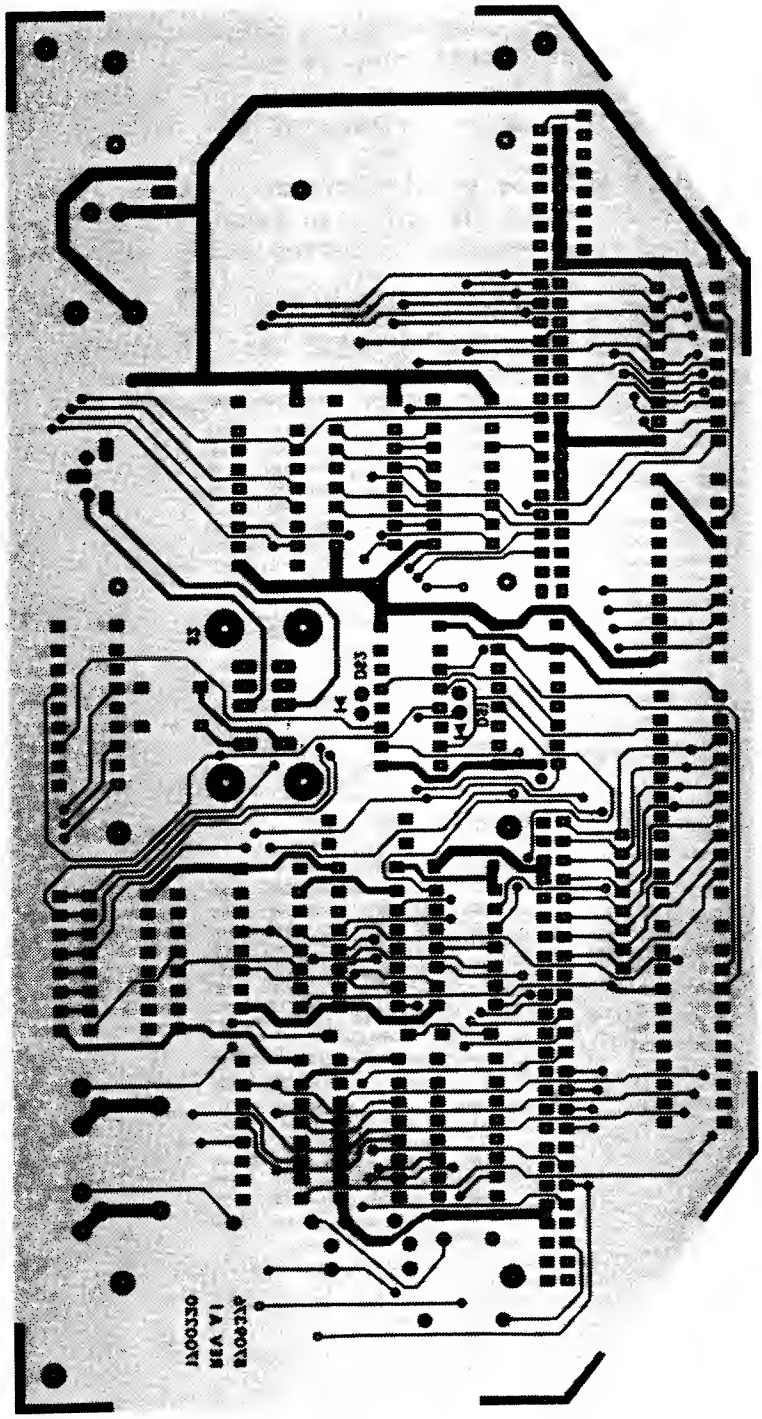
tandy

DWG NO 8000180 — SIZE C — SCALE — SHEET 1 OF 1

PC BOARD LAYOUT



PC BOARD TOP VIEW



PC BOARD BOTTOM VIEW

FDCALG

CHAPTER 6

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MODEL III and Early MODEL 4
FDC ALIGNMENT

General description

"FDCALG3" has been designed specifically for alignment of the FDC board in all Model III's and in the early Model 4's that have the adjustable FDC board. It incorporates self-prompting, user-oriented software.

Operation

The <ENTER> and <BREAK> keys are normally the only keys used. The <ENTER> key advances from one step to the next. The <BREAK> key is used to exit the alignment and return to the main menu and is also used to exit the main menu.

If a diskette with readable sectors is used, a prompt appears for using that diskette after pressing <ENTER> at the main menu. To use it, press <Y>. Pressing any other key is equivalent to a NO response. If the diskette does not have readable sectors, the STATIC alignment procedure will be displayed.

FDC alignment

The FDC alignment consists of two parts, the STATIC and the DYNAMIC alignment. The STATIC alignment is done while the FDC is in a quiescent state (i.e. no commands are being executed) and the DYNAMIC alignment is done while the FDC is executing track write commands.

STATIC alignment
---

1. Adjust R7 to obtain a reading of 1.4 VDC at TP 12, using a DVM.
2. Adjust R6 for a 2.Ø MHZ square wave at TP 13.

Once the static alignment has been done, press <ENTER> to continue.

********** WARNING - THE FOLLOWING PROCEDURE DESTROYS DATA **********

NOTE: The DYNAMIC alignment involves track writes. System and data diskettes that have accidentally been used for this procedure may appear undamaged, but the diskette will be unreliable. DO NOT attempt to BACKUP the diskette. If any data needs to be recovered, COPY it to an undamaged diskette. Even then, the data may be unreliable.

Once the dynamic alignment has been done, the static adjustments should not be repeated unless the dynamic adjustment is also repeated.

DYNAMIC alignment
---

3. The Program will begin writing on track 4Ø. Adjust R5 for 2ØØ nsec precomp pulses at TP 8.

Upon completion of the DYNAMIC alignment, the program may be exited through the following steps:

1. Press <BREAK> - the program will return to the main menu.
2. Press <BREAK> again - a prompt for exiting to TRSDOS will appear.
3. Press <ENTER> - to exit to TRSDOS.

TDC
TANDY DRIVE CONTROLLER

CHAPTER 7

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TDC-DRIVE CONTROLLER DIAGNOSTIC FOR ALL TRS-8Ø 5 1/4 INCH DRIVES

General Description

"TDC" is designed to provide the control signals necessary to align and check-out all of the 5 1/4 inch floppy drives used in TRS-8Ø microcomputers. This diagnostic software is completely menu driven with built-in flexibility to jump from one type drive to another.

Features

1. All types of disk drive can be aligned or checked using the TRS-8Ø Model III, 4, or 4P Microcomputer.
2. Selectable options: drive type, drive step rate, drive sequence and type of test to be performed.
3. Complete flexibility to move between program modules, drive types, step rates, and drive sequence.
4. Built-in timer for timing of work performed.
5. Modules to test: speed, carriage movement, head radial, track zero, index timing, head amplitude, and raw data.
6. Stepping can be elastic or single step.
7. Full informational display giving menu, timer, track, type drive, and step rate selected.
8. Instructions, error messages, oscilloscope connections and oscilloscope settings are displayed as needed in each test module.

Equipment Required

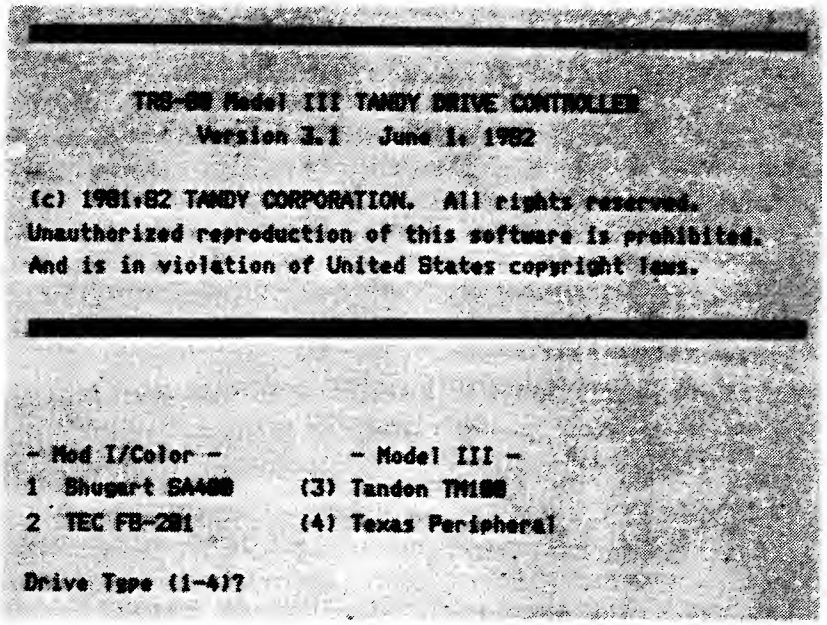
TRS-8Ø Model I or Model III
35 MHz Dual Trace oscilloscope or better
2 scope probes with X1Ø function available
Cable for external sync connection to scope
5 1/4 in. alignment diskette
5 1/4 blank diskette
TDC DIAGNOSTIC PROGRAM

LOADING TDC

1. Power up the computer.
2. Boot the diskette containing the TDC diagnostic program.
3. When "TRSDOS Ready" appears type: TDC <ENTER>.

SELECT TYPE DRIVE

The following message will appear on the screen after Step 3 above:



Type the number key corresponding to the type drive you need to check or align.

For example, if you need to check a Tandon Drive, type the 3 key.

STEP RATE SELECT

After entering a number key the bottom half of the screen will display the following message:

```
(Ø)   6 milliseconds
(1)  12 milliseconds
(2)  2Ø milliseconds
(3)  3Ø milliseconds
(4)  5Ø milliseconds
<ENTER> default rate


Step Rate (Ø-4,<ENTER>)?
```

The operator can select any of the five step rates or the correct "default" step rate will automatically be chosen by pressing the ENTER key.

Default step rates are:

Shugart	3Øms
TEC FB-2Ø1	3Øms
Tandon	6ms
TPI	6ms

NOTE: Insure that the step rate selected does not exceed the fast stepping limit of the selected drive.

Press the key for the step rate desired.

SELECT DRIVE NUMBER

After selecting the step rate, the menu will be displayed with the message in the bottom portion of the screen:

```
Drive to test (Ø-3, <ENTER>=Currently logged drive) ?
```

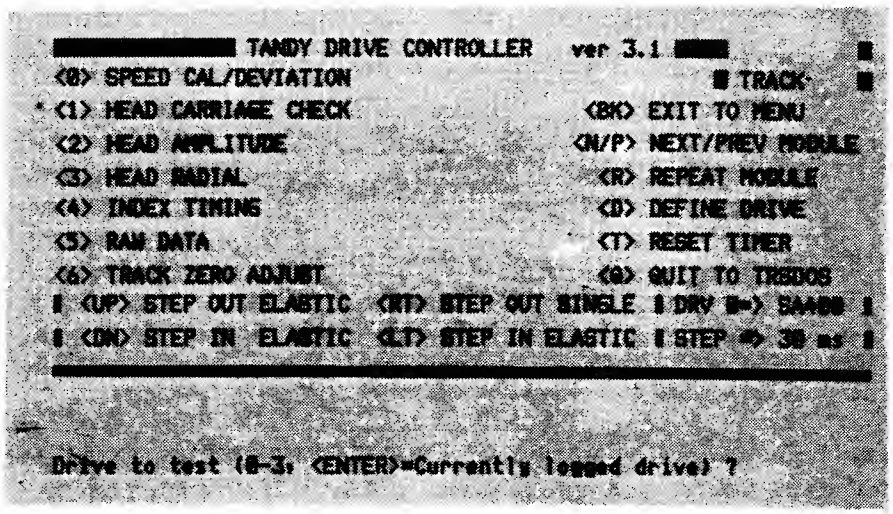
Press the number of the drive position you need to test.
The ENTER key will keep the currently logged drive selected.

MENU DESCRIPTION

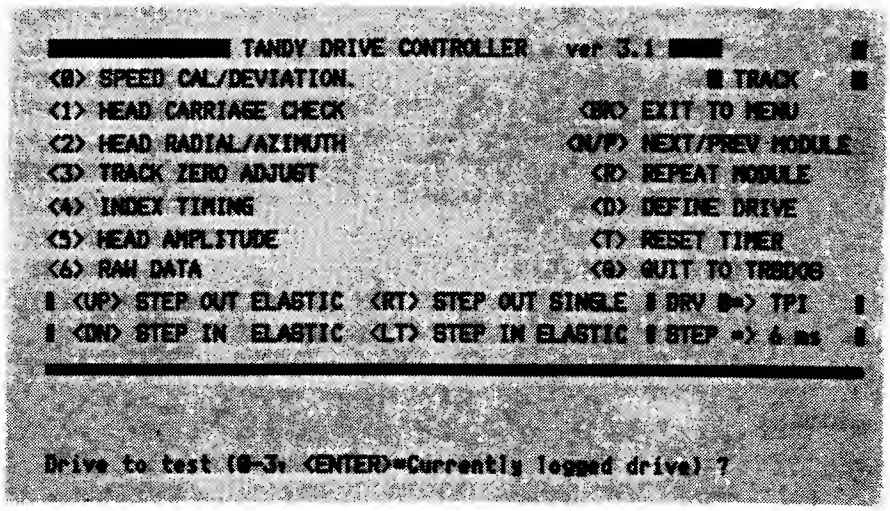
During each test module the bottom section of the screen will be used for:

1. Information about the test in progress,
2. Error message,
3. Messages giving operational conditions,
4. Instructions for performing test, or messages asking for input from the operator.

The top section will contain the following menu when SHUGART or TEC Drives have been selected:



The top section will contain the following menu when TANDON or TPI Drives have been selected:



The menus serves three functions:

1. Information (drive selected, track, time, etc.),
2. Main menu module functions available,
3. Sub-menu modules functions available.

INFORMATION BLOCKS

TIMER

The timer is displayed in the upper right hand corner of the menu section. As soon as the operator enters a drive position number, the timer will start counting time from ØØ:ØØ:ØØ. The timer can be reset to ØØ:ØØ:ØØ by the <T> command on the menu.

The function of the timer is to provide the technician with an indication of the time used in the test and alignment of drives.

TRACK

An display of where TDC believes the current position of the read/write head is provided by the track indicator. This information is necessary in the head radial and track zero adjust modules and helpful in other modules.

DRIVE

The drive block is used to indicate the position of the drive and type of drive selected.

STEP

The step block indicates the step rate currently selected.

SUB-MENU COMMANDS

<BK> EXIT TO MENU

<BK> is used to mean the BREAK key. Pressing the BREAK key during any module will cause an exit of the current module and a return to the main menu.

<N/P> NEXT/PREVIOUS MODULE

During any module, you may return to the previous module by pressing the "P" key or move on to the next module by pressing the "N" key. If the "P" key is pressed in module Ø, control will jump to the main menu. If the "N" is pressed in module 6, control will jump to the main menu.

<R> REPEAT MODULE

During any module, you may restart the module by pressing the "R" key. You will be required to re-enter module entry parameters.

<D> DEFINE DRIVE

Pressing the "D" key will cause an abort of the selected module and jump to the Drive Select Sub-menu command. You can now change the type of drive you are testing. You will also be required to re-enter the step rate and test drive position.

<T> RESET TIMER

If the "T" key is pressed during any module, the timer will reset to ØØ:ØØ:ØØ and restart.

<Q> QUIT TO TRSDOS

Pressing the "Q" key will cause an abort of the TDC program and jump to TRSDOS. This command is useful when ending the test and alignment procedures and another program is to be used from TRSDOS

<UP> STEP OUT ELASTIC

<UP>, which is used to mean the up arrow, will cause the read write/head to step out to track ØØ and back to the starting track. For example, if the head is positioned over track 2Ø and the up arrow is pressed, the head will step to track ØØ and then return to track 2Ø.

<DN> STEP IN ELASTIC

<DN>, which is used to mean the down arrow, will cause the read/write head to step in to the maximum range and return to the starting track. For example, for a Tandon Drive, if the down arrow is pressed when the head is position over track 16, the head will step in to track 39 and return to track 16.

<RT> STEP OUT SINGLE

<RT>, which is used to mean the right arrow, will cause the read/write head to step one track out with no automatic return. For example, if the head is positioned over track 12 and the right arrow is pressed the head will step to track 11 and stay until some other stepping instruction is given.

<LT> STEP IN SINGLE

<LT>, which is used to mean the left arrow, will cause the read/write head to step one step in with no automatic return. For example, if the head is positioned over track 16 and the left arrow is pressed, the head will step to track 17 and stay until some other stepping instruction is given.

MAIN MENU COMMAND DESCRIPTIONS

FOR NORMAL DRIVE ALIGNMENT, ALL MODULES SHOULD BE EXECUTED IN ORDER, Ø-6. MODULE Ø (SPEED CAL/DEVIATION) SHOULD NEVER BE BYPASSED, AS IT AUTOMATICALLY CHECKS THE DRIVE FOR SEVERAL MALFUNCTIONS.

Main menu functions appear on the left side of the video screen, and are selected by responding to the prompt "Test Desired (Ø-6) ?" with the number corresponding to the desired function, or by using the <N> or <P> sub-menu function if already in a module (see sub-menu functions/operation).

Each main menu function consist of a 'module' which is responsible for executing all commands to the disk drive necessary to accomplish the desired alignment procedure. The module also provides prompts for input parameters when required, test equipment setup, test points, and specifications.

SPEED CAL/DEVIATION <Ø> ALL DRIVES

This module is used to check and align the drive motor speed.

When the "Ø" key is pressed to select the Speed Cal/Deviation module, the following message will appear on the screen:

LOAD BLANK DISKETTE, <ENTER>??

This message is prompting the operator to remove any diskettes that contain information and insert a blank diskette. Press the <ENTER> key when a blank diskette has been inserted.

If a write protected diskette is placed in the drive or if the write protect switch is shorted, the LOAD BLANK DISKETTE, <ENTER>?? message will be replaced with the following message:

- ERROR! WRITE PROTECT SHORTED -
<C> CONTINUE, <BK> EXIT TO MENU??

This will allow the operator to place an unprotected diskette in the drive or repair the write protect circuit. The operator can also continue with the test by pressing the "C" key or return to the menu by pressing the BREAK key.

When <ENTER> is pressed after the LOAD BLANK DISKETTE message, self tests are performed automatically on three circuits:

1. Write protect circuit,
2. Track Ø circuit,
3. Index detector circuit.

1. Write Protect Circuit

After the LOAD BLANK DISKETTE message is given, this module samples the write protect bit of the FDC status register until the ENTER key is pressed. When a diskette is inserted in the drive, the write protect switch will go from OFF to ON back to OFF, if the new diskette is not write protected. If this bit does not change before the ENTER key is pressed, the following error message will appear:

- ERROR! WRITE PROTECT FAILURE -
<C> CONTINUE, <BK> EXIT TO MENU??

NOTE: IF A BLANK DISKETTE IS ALREADY IN THE SELECTED DRIVE AND YOU PRESS <ENTER> WITHOUT REMOVING AND REINSERTING THE BLANK DISKETTE YOU WILL GET THIS ERROR MESSAGE.

If the write protect circuits operate correctly, the following message will appear:

- Write Protect Passed -

2. Track Zero Circuit

When the ENTER key is pressed, the drive under test is restored to track zero. The track ØØ bit of the FDC status register is read to determine if the drive track zero circuits are operating. If the track ØØ bit does not change, the following error message will appear:

- ERROR! TRACK ZERO FAILURE -
<C> CONTINUE, <BK> EXIT TO MENU??

If the track ØØ circuits operate correctly, the following message will appear:

- Track Zero Logic Passed -

3. Index Detector Test

When the ENTER key is pressed, the index bit of the FDC status register is read to determine if the index detector circuits are operating correctly. If there is no index pulse from the the drive under test the following message will appear:

-ERROR! INDEX NOT DETECTED -
<C> CONTINUE, <BK> EXIT TO MENU??

CAUTION! DO NOT PRESS THE "C" KEY UNTIL YOU HAVE CORRECTED THE CONDITION CAUSING THE ERROR. IF THE ERROR IS NOT CORRECTED, THE MOTOR SPEED CIRCUITS CANNOT BE TESTED AND THE COMPUTER WILL "LOCK UP" AND MUST BE RESET.

If there is no error in the index detector circuits the following message will appear:

_ Index Detector Passed _

Once the self tests are complete, the program will advance into the RPM mode. In this mode, a motor speed RPM graph, RPM readout, and deviation counters are displayed on the bottom of the screen.

The speed displays in the module are all derived from a software routine that calculates the current drive motor RPM. The software updates the RPM approximately once every 400 milliseconds. If the deviation counters are enabled, they are also updated.

MOTOR SPEED RPM GRAPH

The graph reflects the latest motor speed RPM graphically. A plot is made on the scale for RPM's in the range of 29Ø-31Ø RPM. Any value above or below these values is plotted in the corresponding over-range or under-range portion of the graph.

MOTOR SPEED RPM READOUT

The decimal value of the RPM at last update is displayed to the right of the RPM graph. This value will be constantly changing by one or two RPM's.

DEVIATION COUNTERS

When this module is entered, the deviation counters can be started by pressing the "C" key. The deviation counters will display the maximum and the minimum count. To reset the counters press the "C" key for approximately 1/2 second.

The 1/2 second is required to allow the timers to settle. Failure to observe the 1/2 second time could result in incorrect measurements.

MOTOR SPEED ADJUSTMENT

The motor speed should be adjusted to as near 3ØØ RPM as possible with +/- 4.5 RPM maximum deviation allowed. Each type of drive has a motor speed adjustment as listed below.

	TYPE DRIVE	MOTOR SPEED ADJUSTMENT CONTROL
1.	Shugart SA4ØØ	R-13 on drive motor servo PCB
2.	TEC FB-2Ø1	VR-3Ø1 on drive motor servo PCB
3.	Tandon TM1ØØ	R-4 on drive motor servo PCB
4.	Texas Peripheral (TPI)	R-54 on drive PCB.

HEAD CARRIAGE CHECK

When the head carriage check module is selected, the following message will appear on the bottom section of the screen:

Options:
<ENTER> to AUTO STEP between TRACKS ØØ & **
<U>ser defined AUTO STEP

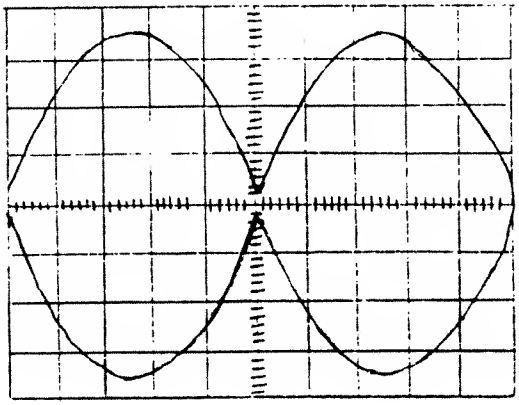
** For Shugart and TEC drives the track limit is 34
For Tandon and TPI drives the track limit is 39

For a normal alignment procedure you should press the ENTER key and allow the drive carriage to step between its maximum ranges. You will be prompted to insert a blank diskette and press ENTER again. The carriage will begin continuously stepping between track ØØ and the maximum track limit.

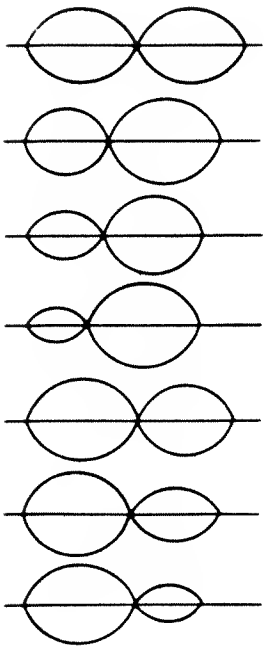
If you wish to step between any other two tracks press the "U" key. You will be prompted to load a blank diskette and press ENTER. After pressing ENTER you will be asked to input a two digit track number. You may select any track within the range of the type drive under test. For tracks Ø - 9 you must enter with a leading Ø such as Ø8 for track 8. After the two digits are entered you will be asked to enter two more digits. These second two digits must be greater than the first two. After the second two digits are entered, the drive will begin stepping between the selected tracks.

While the drive is stepping between track ØØ and its maximum track you should visually observe the carriage assembly to insure that the carriage is moving freely and not binding at any point in its travel. Inspect stepper bands and cam shafts for proper operation. Repair if necessary.

While the drive is stepping, you will be asked to measure the 12V and 5V power supply output. The 12V supply should be 12VDC +/- .6V and the 5VDC supply should be 5V +/- .25V. If the power output is not in tolerance, the power supply should be adjusted, repaired, or replaced to bring it within specifications.



Head/Radial "CATS EYE" Display



Head/Radial Percentages

ALIGNMENT OF HEAD RADIAL

If the head radial is not within specifications you must perform the following steps depending upon the type of drive under test:

SHUGART DRIVE and TEC DRIVE

1. Slightly loosen the two mounting screws for the stepper motor.

2. Turn the stepper motor slightly right or left as needed until the two lobes of the "cats-eye" are as nearly equal as possible.

NOTE: IF YOU MOVE THE STEPPED MOTOR TOO FAR ONE DIRECTION THE RIGHT LOBE WILL COMPLETELY DISAPPEAR AND TOO FAR IN THE OTHER DIRECTION THE LEFT LOBE WILL COMPLETELY DISAPPEAR. WHEN EITHER OF THESE CONDITIONS EXIST, THE STEPPER SYSTEM IS AT LEAST ONE FULL TRACK OFF TRACK 16.

3. After Step 2 above, tighten the mounting screws for the stepper motor while watching the "cats-eye" to insure that the pattern does not change.

4. Use the "UP" arrow to step out elastic. Verify that the head radial is still within specifications. Re-adjust as necessary.

5. Use the "DOWN" arrow to step in elastic. Verify that the head radial is still within specifications. Re-adjust as necessary.

6. Repeat Steps 4 and 5 until the "cats-eye" pattern remains within specifications after stepping in and out elastic.

7. Insure that the stepper mounting screws are tight.

TANDON DRIVE and TPI DRIVE

1. Loosen the two retaining screws on the rear of the unit, and the retaining screw on the carriage assembly.

FINE ADJUSTMENT

2. While observing the scope, turn the adjustment screw until the lobes are of equal amplitude.

COURSE ADJUSTMENT

3. If the fine adjustment will not bring in the lobes to nearly equal size, loosen the hex screw on the stepper motor collar and adjust the lobes to the proper pattern by rotating the cam. Then repeat the fine adjustment above.

4. Tighten all retaining screws.

5. Use the "UP" arrow to step out elastic. Verify that the head radial is still within specifications. Re-adjust as necessary.

6. Use the "DOWN" arrow to step in elastic. Verify that the head radial is still within specification. Re-adjust as necessary.

7. Repeat Steps 4 and 5 until the "cats-eye" pattern remains within specifications after stepping in and out elastic.

8. Insure that the retaining screws are tight.

AZIMUTH CHECK

Field adjustment of azimuth is not possible at this time, and is NOT supported!!! This module is included for upward compatibility purposes only.

TRACK ZERO ADJUST

This module will allow you to check and adjust the track zero switch. In the information section of the screen you will be given instructions for connecting your oscilloscope to the type drive that you are testing. The test points used differ between drives; therefore, make sure that the drive under test is the same as that shown in the drive section of the screen.

**********CAUTION**********CAUTION**********

BEFORE INSERTING YOUR ALIGNMENT DISKETTE INSURE THAT THE WRITE PROTECT CIRCUITS ARE OPERATING PROPERLY ON THE DRIVE UNDER TEST. IF THE ALIGNMENT DISKETTE IS ACCIDENTALLY WRITTEN ON OR ERASED IT WILL BE UNUSABLE.

**********CAUTION**********CAUTION**********

Insert the alignment diskette when prompted.

Follow the instructions for setting up and connecting the oscilloscope.

TRACK 16 CONFIRMATION

The first step of the Track Zero Module is to insure that the head radial "cats-eye" is found on track 16. It is possible to have the track zero switch exactly four tracks off; however, if this condition exists, the "cats-eye" would not be found 16 tracks from the incorrectly set track zero switch.

NOTE: THE ALIGNMENT DISKETTE HAS THE CATS-EYE RECORDED EXACTLY ON TRACK 16. IF THE TDC TRACK INDICATOR DISPLAYS ANY OTHER TRACK OTHER THAN 16 WHEN THE CATS-EYE IS PRESENT, THERE IS AN ERROR IN THE TRACK ZERO ADJUSTMENT OR MALFUNCTION OF THE HARDWARE.

Observe the oscilloscope display. When the read/write head is positioned on track 16, the display should be a "cats-eye" pattern with each "eye" being of equal size. If no "cats-eye" is observed on track 16, single step to track 12. If the pattern is now present, you will have to move the track zero switch out four complete tracks before the fine adjustment.

TRACK ZERO ADJUST

Set the oscilloscope controls and connections as directed by the display.

The signal on the oscilloscope screen should be a rectangular wave with a 50% duty cycle. If the signal does not have a 50% duty cycle you must:

1. Slightly loosen the track zero mounting screw.

2. While observing the track zero signal, move the track zero switch until the waveform has a 50% duty cycle.

3. Hold the switch in position and tighten the mounting screws.

TRACK ZERO CONFIRMATION

After verifying the track zero 50% duty cycle, press <ENTER>. You will now be prompted to reconfigure the oscilloscope to monitor the signal recorded on track zero of the alignment diskette. Set up the oscilloscope according to the instructions.

If the read/write head is positioned on true track zero, you will observe a data pattern on the oscilloscope.

TANDON and TPI TRACK ZERO STOP ADJUST

1. Back off the track zero screw two turns.

2. Slowly turn the track zero stop screw in until the output amplitude starts to decrease.

3. Back the track zero screw out until the amplitude stops increasing. Turn the screw out another 1/2 turn form this point.

INDEX TIMING MODULE

This module allows you to set the index sector assembly so that the index signal will occur just prior to the start of data recording.

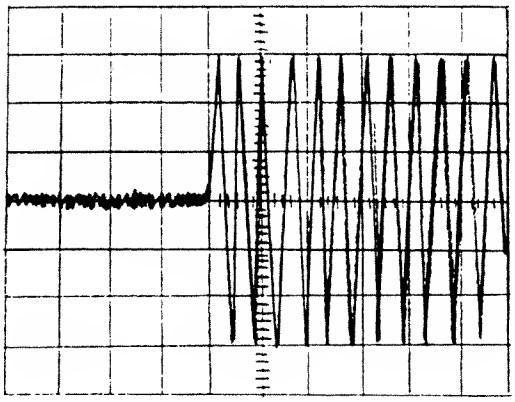
After selecting this module, set the oscilloscope controls and connections according to the instructions on the display.

The external sync signal is generated each time the index hole in the diskette passes the index assembly. There is a data burst recorded on track 1 of the alignment diskette. This data burst should occur on the scope 2ØØ microseconds after the start of the sweep.

NOTE: IF THE DATA BURST SHOULD BE OUT OF ALIGNMENT SUCH THAT IT OCCURS EARLIER OR MORE THAN 5ØØus LATER THAN THE INDEX SYNC PULSE, YOU WILL HAVE TO SLOW DOWN THE TIMEBASE UNTIL YOU CAN SEE THE DATA BURST.

To adjust the index timing you must:

1. Slightly loosen the mounting screws of the index assembly.
2. Move the index assembly until the data burst is 2ØØ microseconds from the start of the sweep. You are allowed +/- 5Ø microsecond tolerance; however, you should adjust as near to 2ØØ microseconds as possible.
3. Hold the index assembly in place and tighten the mounting screws.



Index Timing Display

HEAD AMPLITUDE MODULE

In this module you will be observing the amplitude of the read head circuits. Each type of drive has different minimum head amplitude.

Shugart - 200 mv
TEC - 300 mv
Tandon - 225 mv
TPI - 200 mv

After selecting the Head Amplitude Module, you will be asked to enter the data pattern to write. Normally you will press the <ENTER> key for a pattern of FF. If you want any other pattern enter the Hex code of the desired pattern.

Next you will be asked the track on which you are to write the selected data pattern. Normally you will press <ENTER> for track 34. If you want to write on any other track enter its two digit decimal number.

You will be asked to enter the write mode. Normally you will press <ENTER> for a single write. If you need a continuous write press the "C" key.

Next you will be asked to select the FDC density. If you want to use single press <ENTER> or if you want double press the "2" key.

WARNING: YOU MIGHT FIND SOME EARLY MODEL SHUGART DRIVES THAT WILL NOT ACCEPT DOUBLE DENSITY DATA. ALSO, DOUBLE DENSITY WILL WORK ON A MODEL I ONLY IF THE DOUBLE DENSITY ADAPTER HAS BEEN INSTALLED.

The instructions and specifications for the type drive selected will now be displayed. Set the scope connections and controls as instructed on the display.

NOTE: THE TPI PCB USES DIFFERENT TEST POINT NUMBERS. BE SURE THAT YOU USE THE CORRECT TEST POINTS.

If the head amplitude is not above the minimum for the type of drive under test, you must do one of the following:

1. Clean the read/write head.

2. Try different media.

3. For Shugart Drives, replacing the head load pad could increase head amplitude.

4. For the other type drives, replacing the head load arm could increase head amplitude.

5. Repair/replace logic board.

6. Replace read/write head assembly.

COMPLIANCE CHECK

The compliance check is useful to determine if the pressure of the head load pad against the media is sufficient.

Apply an additional 15 grams (the weight of a quarter) to the head load arm. By observing the head amplitude, verify that the voltage did not increase by more than 10%.

If there was an increase of more than 10%, you must take the following action:

1. For Shugart Drives, replace the head load pad.

2. For TEC Drives, replace the head load arm.

3. For Tandon and TPI Drives, loosen the two nuts that holds the load arm to the carriage assembly. While observing the scope, move the arm until the output is highest. Hold the arm in this position and tighten the nuts.

4. Re-verify the compliance after corrective action is completed.

RAW DATA MODULE

The Raw Data Module is a check of the mechanical and electrical effect on the data being read from the media. Mechanical jitter could be caused by:

1. Drive belt
2. Drive motor
3. Motor control circuits
4. Hub wear
5. Hub bearings
6. Enlarged center hole on media

Electrical jitter could be caused by:

1. Logic PCB
2. Read/write head

After selecting the Raw Data Module you will be asked what data pattern to write. Normally you will select a pattern of FF by pressing the <ENTER> key. If you need some other data pattern you can enter the two hex digits of that data pattern.

Next you will be asked to select the FDC density. For single density press <ENTER>, for double density press the "2" key.

WARNING!! YOU MIGHT FIND SOME EARLY MODEL SHUGART DRIVES THAT WILL NOT ACCEPT DOUBLE DENSITY DATA. ALSO, DOUBLE DENSITY WILL NOT WORK ON THE MODEL I UNLESS THE DOUBLE DENSITY ADAPTER HAS BEEN INSTALLED.

Follow the instructions given for connecting and adjusting the scope. You must use an erased blank diskette for this check.

NOTE: YOU ARE ONLY USING ONE CHANNEL OF VERTICAL INPUT IN THIS CHECK. YOU MUST DISCONNECT THE UNUSED PROBE FROM THE DRIVE.

There will be adjustments for electrical jitter on the TPI and Shugart drives. On the TEC and Tandon there is no adjustment.

1. For the Shugart Drive, adjust R13 on the PCB for centering of the 2nd pulse between the 1st and 3rd pulse. There should be no more that 300 nsec jitter on the 2nd pulse.

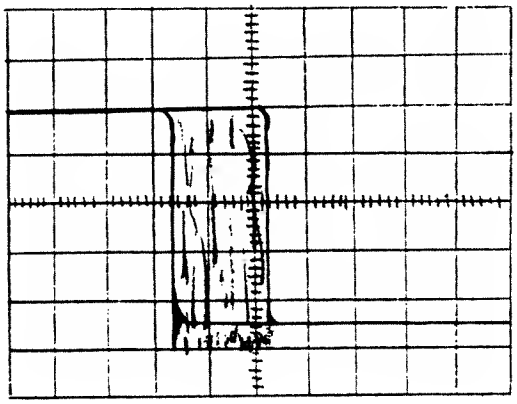
2. For the TPI Drive, adjust R23 on the PCB for centering of the 2nd pulse between the 1st and 3rd pulse. There should be no more than 240 nsec jitter on the 2nd pulse.

NOTE: "JITTER" IS MEASURED AS THE WIDTH OF THE RISING OR FALLING PULSE TRANSITION, WHICH APPEARS AS THE BLURRED AREA.

3. On the Tandon and TEC Drives you can only check for centering of the 2nd pulse between the 1st and 3rd pulse.

If the electrical jitter cannot be brought to specifications, you will need to repair/replace the PCB or replace the read/write head.

If the 3rd pulse jitter is more than 48Ø nsec on any drive, the problem is probably caused by an item from the mechanical jitter list on the previous page.



Raw Data "Jitter"

TDC ERROR MESSAGES

TDC error messages are generated by the TDC program upon the detection of specific failures. The error checking is automatic, and the user is notified of the status as each test is completed. Whenever an error code is generated, the noted defect should be corrected before continuing further service or alignment procedures.

The following error code list states the reason the error was detected, and possible problems causing the failure.

ERROR! WRITE PROTECT SHORTED

Indicates that the write protect switch is shorted, remaining closed due to mechanical problem, or that the write protect electronics are outputting a constant logic high to the FDC.

ERROR ! WRITE PROTECT FAILURE

The write protect switch status is failing to toggle when a non-write protected diskette is inserted in drive. Switch may be open, maladjusted, the switch arm may be broken, or write protect electronics are outputting a constant logic low to the FDC.

ERROR! NO DISKETTE IN DRIVE

No diskette was in drive when required by program. Checked only in modules that write to diskette.

ERROR! DOOR NOT CLOSED

Disk drive door was not closed when required by program.

ERROR! DISKETTE IS WRITE PROTECTED

A write protected diskette was inserted during a step that writes to the drive. For your protection, write protect TDC program diskettes!

ERROR! INDEX NOT DETECTED

Index pulse (IP*) is not being sensed by FDC. Possibly defective index assembly, or index electronics logic failure.

ERROR! CANNOT FIND TRACK ZERO

Track zero signal (TRKØØ*) is not being sensed by FDC. Suspect bad track zero switch alignment, defective track ØØ switch, or track zero electronics logic failure. Less likely: defective stepper motor, stepper motor control logic failure, or suspect 12 volt supply failure.

DISKDG5

5 1/4 - INCH DRIVE DIAGNOSTIC PROGRAM

CHAPTER 8

```
**************************************************************************
***** WARNING!  WARNING!  WARNING!  WARNING!  WARNING!  WARNING! *****
**************************************************************************
*****                                                                *****
*****        THIS PROGRAM CAN DESTROY DATA!!!   BE CAREFUL           *****
*****         AND BE CERTAIN YOU UNDERSTAND HOW TO USE IT            *****
*****            BEFORE ATTEMPTING TO USE IT FOR DRIVE               *****
*****               VERIFICATION OR TROUBLESHOOTING                  *****
*****                                                                *****
**************************************************************************
```

DISKDG5 - Drive Reliability Test for 5 1/4 - inch Disk Drives

Table of Contents

DISKDG5 5 1/4 - inch DISK DIAGNOSTIC

INTRODUCTION

DISKDG5 is intended to assist in the troubleshooting of 5 1/4 inch disk drives.

GENERAL DESCRIPTION

"DISKDG5" is designed to test all types of 5 1/4 inch floppy disk drives currently used in the TRS-80 Model III/4/4P and Model 2000 Microcomputers. The program uses a menu drive that allows the user to change drive parameters and to select several different test modes. The user can select a programmable number of passes for 1 to 4 drives at a time, or a continuous mode can be selected.

FEATURES

All 5 1/4 inch drives can be tested with the same program.
Menu drive gives all available options at a glance.
Cumulative errors may be viewed after each test and may also be sent to the line printer.
Complete history of each drive maintained and may also be sent to the line printer.

EQUIPMENT REQUIRED

TRS-80 Model III, 4 or 4P.
5 1/4 inch formatted diskettes for each drive being tested.
For 80 Track drives - drive cable with pin 32 installed on the FDC connector and on the drive connector (pin 32 is side select).
"DISKDG5" DIAGNOSTIC PROGRAM.

PREPARING DRIVES FOR TESTING

35 TRACK DRIVES

The 35 track drives (Shugart and TEC) can be tested using diskettes formatted with FORM35 or with diskettes formatted on 40 track drives using the standard TRSDOS formatter.

40 TRACK DRIVES

The 40 track drives (Tandon and TPI) are tested using standard TRSDOS format.

80 TRACK DRIVES

The 80 track drives (Mitsubishi) can be tested by formatting them using LDOS. To format with LDOS, boot up an LDOS diskette, insert a blank diskette in the drive to be formatted and type:

FORMAT :d (NAME="TEST",MPW="PASSWORD",DDEN,SIDES=2,CYL=80) <ENTER>.

Once all test diskettes have been formatted, boot up the diagnostic diskette and execute DISKDG5.

OPERATING DISKDG5

This diagnostic is for testing all 5 1/4 inch disk drives.

To start the program type <DISKDG5> <ENTER>. You will then be prompted to remove the system diskette. The test should not be started until the system diskette is removed in order to prevent accidental damage to the system diskette. After the test has been started, this module will not be repeated unless the test is re-started from TRSDOS Ready.

After pressing <ENTER> the main menu will appear.

MENU DISPLAY

The main menu is in two sections. The first, at the top, displays enabled drives, drive type, test mode and read/write status. Any or all of these may be altered using one of the menu options. The second part of the display lists the menu options, preceded by the key to press to select that option.

<0-3> - Enable / Disable Drive

To enable a drive for testing, simply press the number of the desired drive (i.e. to enable drive 2 press <2>). Pressing the same key again will disable that drive and it will not be tested. As a drive is enabled, its number will appear at the top beside "Drives:". When disabled, its number will be blanked out.

<D> - Select Drive Type

This menu option allows the user to select any 5 1/4 inch drive currently being used in the TRS-80 Models III, 4, 4P and Model 2000. Drive type will determine step rate, number of tracks and sides automatically.

<M> - Mode

This option allows the user to select either a specified number of passes or continuous testing. Enter either a number in the range 0 to 255 or a "C". If a number is entered, each drive will be tested for that number of times and then the next drive is tested. After all drives have been tested for the selected number of times, the menu display will return. If continuous ("C")

is selected, each drive will be tested once before the next drive is tested and then the test will re-cycle back to the first drive.

<W> - Toggle Read / Write

This option allows the user to select whether to write to the disk before reading. The program initializes to "Read Only" in order to prevent accidental destruction of data. When testing, it is recommended that the Read/Write option be used.

<A> - Read / Write All Tracks Sequentially

This test option tests each track on all enabled drives sequentially.

<R> - Read / Write Random Tracks

This test option causes the drive to do long seeks between tracks. All tracks will be tested, although not in sequential order. This option will provide the most thorough testing of the drive.

<S> - Read / Write Some Tracks

This option provides a quick test of the outermost, middle and inner tracks.

NOTE - THIS IS NOT A THOROUGH TEST! It is intended only as a quick check to see if the drive is at all functional.

<T> - Read / Write a Selected Track

This option allows repeated testing of one track. Upon selecting this option, the user is prompted for a track number for testing.

<H> - Drive(s) History

This option allows the user to view the cumulative errors on each drive and the drive history by track number on each drive.

TEST DISPLAY

The test display shows the current drive under test. The pass mode shows the number of passes to be executed and the pass count displays the number of passes completed. If continuous mode was selected, the pass count will reflect the total number of cycles completed.

The sector count will not be sequential (1,2,3...18) on TRSDOS formats. DISKDG5 uses a skip factor of 3 instead of TRSDOS's skip factor of 6. This makes the test run faster and puts more stress on the drive. LDOS format used on the 80 track drives uses an interleave of 3 and so the sector count (0..17) will be sequential when testing those drives.

If a fatal error occurs during the test, the test will abort on that drive and continue on to the next enabled drive or return to the menu if no other drive is enabled. For an explanation of fatal errors see EXPLANATION OF ERRORS.

While a drive is being tested, the test can be exited by pressing <BREAK>. This will return you to the main menu after any in-progress sector read or write has been completed. Hold the break key until the menu appears.

CUMULATIVE ERRORS

After completion of the test, or after pressing <BREAK> during a test, the main menu will again be displayed. To see the cumulative errors (total errors for each drive) press <H>. The total number of errors will be displayed along with the pass number on which the first error occurred. If no fatal errors occurred, the pass that the first non-fatal error occurred will be displayed. If a fatal error occurred, the pass that it occurred on will be displayed regardless of any prior non-fatal errors.

To return to the main menu, press <BREAK>. Pressing <P> will output the errors to the printer. Pressing a drive number (0 - 3) will display the history for the drive.

DRIVE HISTORY

The history tables can be accessed from the cumulative error display. To view the history on a particular drive, press the number of the drive (e.g. press <2> to view the history on drive 2).

At this point, you are prompted to select either the video screen or the printer for output. Pressing <P> will output the table to the printer,

pressing <S> will output it to the screen. The scrolling of the display can be halted by pressing the <SPACE> bar and restarted by pressing <ENTER>. After halting the display, one track at a time can be displayed by pressing the <SPACE> bar again.

If a double-sided drive has been tested, the errors for side 0 will be displayed first, followed by the errors for side 1. After the entire history of the drive has been displayed, you are asked if you wish to re-display the errors. If you answer <N>, you will be asked if you wish to clear the table. Pressing <Y> will clear the table, pressing <N> will leave the table as it is.

NOTE - If the table is not cleared, any further testing on that drive will add errors to those already existing.

Answering <Y> to the clear history prompt only clears the table for that selected drive. The other drive histories will be left unchanged. To clear all of the tables, each history table must be individually selected. All the tables are cleared only on INITIAL start-up.

EXPLANATION OF ERRORS

NON-FATAL ERRORS - these errors do not interrupt testing:

READ ERRORS - this counter is incremented whenever an error occurs during a read command.

WRITE ERRORS - this counter is incremented whenever an error occurs during a write command.

SEEK ERRORS - this counter is incremented whenever the drive was unable to find the next track to be tested.

CRC ERRORS - this counter is incremented whenever the CRC (cyclic redundancy check) did not match the checksum of the current sector. This indicates that the data field is not correct or was read incorrectly.

RNF ERRORS - this counter is incremented whenever the designated sector was not located.

FATAL ERRORS - these errors cause an abort of testing:

DRIVE NOT READY - this error indicates that the READY signal to the FDC is a logic 0. The FDC will abort any seek, write or read

operations in this case.

WRITE PROTECT - this error indicates that the disk is write-protected and the FDC will abort any write commands. This error is only fatal in the READ/WRITE mode. In the READ ONLY mode, the test will continue.

LOST DATA - this error indicates that the CPU did not pick up the last byte read in time on a read operation or did not send a byte in time on a write operation.

HARD DISK DIAGNOSTIC
HDDIAG

CHAPTER 9

TABLE OF CONTENTS

INTRODUCTION

The following program is provided to assist in the alignment and troubleshooting of the Model I/III Five Megabyte Hard Disk System:

HDDIAG

```
************************************************************
**** WARNING!  WARNING!   WARNING!   WARNING!  WARNING!  ***
************************************************************
****                                                    ****
****   THIS PROGRAM CAN DESTROY DATA!!    BE CAREFUL    ****
****   AND BE CERTAIN YOU UNDERSTAND HOW TO USE IT      ****
****       BEFORE ATTEMPTING TO USE IT FOR DRIVE        ****
****        VERIFICATION OR TROUBLESHOOTING!!!!!        ****
****                                                    ****
************************************************************
```

GENERAL DIAGNOSTICS PRECAUTIONS:

1. Do not attempt to transfer this diagnostic to other versions of TRSDOS or other Disk operating systems!! Boot the diagnostic with TRSDOS by turning the Computer on, inserting the diskette in drive Ø, closing the door, and then hitting the reset button.

2. There will be some bad blocks on the Hard Drives. While the Operating System does not use and ignores them, they will be detected by the diagnostics!! DO NOT ASSUME THE PLATTER IS DEFECTIVE BECAUSE THE DIAGNOSTIC DETECTS A BAD BLOCK! Check the chart supplied with the drive to verify which blocks are bad on the drive you are testing.

QUICK REFERENCE SECTION

Execution:

1. Type <HDDIAG3> and <ENTER>
2. Type <ENTER> again to map the controller board at Port ØCx hex.
3. Select drive number to test.

Description: This program tests and manipulates various Hard Disk controller circuitry. Option <A> provides a method for adjusting the controller VCO and "DRUN".

OPTIONS:

<T> The Task and Control registers are written to and then read from to verify proper register operation.

<O> Restores the drive to track Ø (cylinder Ø, head Ø)>

<S> Allows user to seek a specified track with optional seek verification.

<C> Allows user to step heads between two selected tracks.

<L> Steps the heads from outermost to innermost tracks in decreasing order. Exercise operation of slew step rate changes.

<M> RAM test for the static 2114 15Øns RAMS on the controller.

<I> Seeks current track to generate an interrupt. Verifies that interrupt is received.

<D> Selects drive number to test.

<A> Self-prompting controller board alignment procedure.

<G> Reads and displays controller status from the previous operation.

<X> Generates random track number, reads a random sector on that track, and checks the status register for errors.

<R> Reads current track, checks status register for errors.

OPTIONS (continued)

<W> Writes to currently selected track, checks for errors.

```
**************************************************
***  WARNING!!! THIS OPTION WILL DESTROY CUSTOMER   ***
***  DATA IF A CYLINDER OTHER THAN THE DIAGNOSTIC   ***
***  CYLINDER (Tracks 4,5,6,7) IS WRITTEN.         ***
**************************************************
```

<F> Formats Diagnostic Tracks (track 4,5,6 or 7 which ever was used last) and checks for errors. This test does not interfere with customer data, providing head position and head select are functioning properly.

<P> Reconfigure the program. Allows the user to change the step rate, sector size, number of heads, the use of interrupts, and the number of cylinders.

<Q> Exit to TRSDOS.

TECHNICAL SECTION

HDDIAG3 consists of tests which exercise the Hard Disk controller and Drive assemblies. The flexibility of the tests provides a method for categorically isolating faults in the controller or drive assembly.

Features have been implemented to safeguard the customer's data. Cylinder 1 on each drive is designated as a "Diagnostic Cylinder". Read and write loop testing may be done on tracks 4,5,6, or 7 (Cylinder 1) without concern for the customer's data. In the event that a fault causes the destruction of the diagnostic track ID field, the <F> option allows reconstructing the diagnostic track. Use the <S>eek without verify to select the appropriate track.

Even with these features, ALWAYS BE CERTAIN THAT THE CUSTOMER HAS BACKED UP THE DATA FILES IF AT ALL POSSIBLE before servicing the drive!!!!

Options:

<T> Task Register

The Task Register test provides several modes of operation. The Single test mode allows the test to run through once, while the Loop Test Mode allows continuous exercising of the test for signal tracing with a scope.

The registers are addressed at ports C1 and CA-CE hex. The logic pattern which is written and read is a rotating "logic 1" in a field of "zeros", followed by a rotating "logic Ø" in a field of "ones". This provides a means of testing the control register and controller. The input buffers for the read & write control functions, the data lines & data access lines internal to the controller board, and the chip enable function are all required to operate in order for this test to pass. The test will display "TASK REGISTER TEST PASSES" if all the required signal paths are good. If there is a mismatch of data written & read, then the difference is shown as the address and data byte, one error at a time. Pressing any key will advance the test.

If the control register, the task register or supporting circuitry is defective, then no commands required to operate the drive can be executed properly.

<M> Static RAM Test

The static RAM's (U-17, U-18) provide the I/O buffer for data transfers to/from the Hard Disk. The Hard Disk is formatted with 256 byte physical sectors, so 256 bytes of the static RAM are used to buffer the data between the host and the Hard Disk.

The Hard Disk host computer is not capable of keeping up with the high data rate required for Hard Disk read/write operations. For this reason the host computer interfaces through the static Ram buffer with the data to transfer. In addition, the 8X3ØØ microprocessor uses approximately 2Ø bytes of the RAM as a "scratchpad".

The Static RAM test exercises the buffer area of the RAM, but not the scratch space - It is not available to the host computer. Additionally, the RAM's are in parallel, and therefore affect each other. Due to these limitations in testing the RAM's, the test may not always detect a fault. If Static RAM problems are suspected, it may be wise to substitute "known good" RAM's (Remember - 15Ø nanosecond RAMs are required!).

<I> Interrupt Test

The interrupt test checks the ability of the controller to generate an interrupt enable/disable option.

The current interrupt status is displayed on the right side of the status line. Note that the interrupt test enables the interrupt mode, runs the test, then restores the interrupt mode back to its initial condition.

The actual command executed to cause the interrupt is a seek of the current track on which the selected Hard Disk is positioned. The interrupt test fails if the interrupt service routine is not executed within several seconds, and a appropriate failure message is displayed on the video screen.

<S> Seek Track

The Seek Track option requires 4 digits for the track number in the range of ØØØØ to the maximum set by the configure <P>rogram command. This is the track number and NOT the cylinder number. You may seek with a Read Verify to ensure that the drive found the target track, or select not to verify to determine if the drive can seek a track independent of a read operation. The default is No Verify. Also, 4 digit track numbers must be used.

<C> Carriage Step

Carriage Step allows the entry of two track numbers to step between. Four digits are required, and you must enter the low track number first. The seeks are accomplished without a read verify. Note that seeking between tracks on the same cylinder will not cause a step - just an alternate head to be selected.

<L> Slew Seek Test

The Hard Drive employs slew seeking to optimize step rates. On long distance seeks, the step rate is actually done at a higher rate than for short seeks.

The test causes the head assembly to seek the extreme tracks, then moves toward the middle tracks, and then toward the extreme tracks again. This provides a method of exercising the slew seek feature of the drive and operates the circuitry for scope probing in the event of a failure in this area.

<R> Read Current Track

This command reads the current track on which the head is positioned, either in the interrupt mode or the polled status mode. LDOS software uses the polled status mode for all hard disk I/O.

The interrupt mode is faster than the polled status mode. If the interrupts are not functional, then the speed of reading the sectors will slow down and a "NO INTERRUPT RECEIVED" error message will be displayed. The speed of reading the track is proportional to the accuracy of the controller VCO tracking the data rate. The controller does 16 retries, auto restores at a slow step rate, then performs 16 more retries before exiting with an error status when invalid information is encountered.

<W> Write Current Track

The Write Current Track option uses the Z8Ø 'R' (refresh) register to generate the random data to be written on sectors 1 through the maximum set by configure <P>rogram minus 1 (LDOS uses sector number Ø-31 and this program uses sector numbers 1 to one less than set by configure <P>rogram) of the track on which the head is positioned. The program warns of the possibility of destroying customer data, and requires a "Y" (yes) response to continue. The routine checks for a write protected hard drive. The program will not normally allow a write on a drive with a write protect condition. HOWEVER, IN A FAULT ENVIRONMENT THERE ARE NO GUARANTEES. It is best to attempt a write on the "Diagnostic Cylinder" (cylinder 1) to check the write protect function.

<X> Random Read

The Random Read test is the most demanding test. The target track to be read is displayed on the video as the routine runs. A random sector in the range of 1 to one less that the number set by configure <P>rogram is read and implied seeks are utilized.

ALIGNMENT PROCEDURES

HARD DISK MOTOR SPEED ADJUSTMENTS

(5" Tandon Hard Drives only)

```
**************************************************************
*    WARNING  WARNING  WARNING  WARNING  WARNING  WARNING    *
*    The bubble can be operated on its side but it should    *
*              NEVER be operated upside down.                *
**************************************************************
```

Motor speed alignment is very important for proper operation of the Hard Drive and should be done before attempting to align the controller board. Each Hard Drive in the system should be checked for correct motor speed. This can be accomplished with the diagnostics and a frequency counter. Select the first Hard Drive with the diagnostics and place the frequency counter probe to test point 3 on the drive logic board. The counter should display a count of 16.58ms to 16.74ms. If the count is not within this range motor speed alignment is required and you should proceed to step one. If the count is in this range DO NOT attempt to adjust it.

NOTE: If more than one Hard Drive is in the system, you will need to select each Hard Drive individually and check motor speed as above.

1. With power off, remove the four screws that hold the metal frame the controller board and power supply are mounted on. Disconnect the cables from the bubble assembly to the controller board, and tilt the controller board and frame to the right up on its end. This way the power supply can still be connected to the bubble assembly.

2. Remove the four screws that hold the bubble assembly brackets to the base of the hard disk and turn the bubble assembly on its left side so the drive logic board is facing the power supply.

3. Remove the right bubble mounting bracket (which should now be on the top of the bubble) to expose the holes which allow access to the motor speed adjustment pots.

4. Be sure the drive logic or any other boards are not shorting to the frame and turn on the power.

5. Attach the Frequency Counter probe to Test Point 3 of the drive logic board. Adjust R5 for a 16.58ms to 16.74ms count.

6. Power down and reassemble.

5 INCH HARD DISK ALIGNMENT PROCEDURE

For 8X3ØØ type boards

The hard disk controller board adjustments need to be done only on the primary hard drive. The motor speed will need to be adjusted on each hard drive in the system.

Alignment of the 5" Hard Drives has become very important for proper operation. The following are the procedures you should follow in doing these alignments.

MINIMUM EQUIPMENT REQUIRED:

6Ø MHZ Oscilloscope (Tektronics 2213 or B&K 157Ø)
Plastic tunning tool
x1Ø scope probes
HDDIAG Diagnostics diskette

NOTE: 1. A MINIMUM 6Ø MHZ scope must be used.
2. DO NOT use a metal screwdriver for the adjustments as it can affect the circuit under test.
3. DO NOT use xl scope probes as they can load down the circuit under test.

HARD DISK CONTROLLER BOARD ADJUSTMENTS

There are three adjustments on the controller board. R1 adjusts the one shot used to start the reading of the track. R18 adjusts the bias on the error amplifier. C33 adjusts the free running frequency of the VCO.

Run the program HDDIAG and proceed to step 1 of the alignment procedures for 5" hard drives. Before starting this procedure, the drive should be running for about 5 minutes.

1. Voltage controlled oscillator (VCO) adjustment.

First check for between +2.4 to +3.Ø Vdc at pin 14 of U32. If it is not within this range, check R22, R24, and U32. R22 and R24 form a voltage divider to supply a reference voltage to U32. If the voltage is not within this range, either one of the resistors has an incorrect value or U32 is pulling down or in some other way affecting the voltage.

Then attach Channel A of your scope to TP9 and set Channel A to 2 volts/div. TP9 is between U33 and U34.

DC couple Channel B, set it to 1 volt/div. and attach it to TP8. TP8 is between the voltage regulator and U32.

The time base should be set for 5Ø nanoseconds/div.; trigger should be normal and on channel A. The scope should be set to dual trace mode to display both channels simultaneously.

Adjust C33 and R18 to obtain exactly a 1ØØ nanosecond period waveform on Channel A and a +2.5 Vdc level on channel B. You should have your scope set up to display both of these signals at the same time. Adjusting one will affect the other. See Figure 1.

When this has been done press enter to proceed on to the next step.

2. "DRUN" adjustment

DC couple Channel A and connect the probe to TP1. TP1 is located between U1 and U2. The timebase should be set to 5Ø nanoseconds/div. and trigger should be set to negative and normal.

R1 should be adjusted so that Channel A's waveform is clean and low for 25Ø +/- 5 nanoseconds. After the 25Ø nanoseconds, the signal will look like garbage (that is, both high and low at the same time). This is normal. See Figure 2. Once you have adjusted for the proper DRUN signal you need to make sure the signal is truly "locked" in. This can be accomplished by turning the Hard Disk off, wait 3Ø seconds, then turn the Hard Disk back on again and verify the signal has not changed. This step is very important as it is possible to have the proper signal displayed on the scope but as soon as you turn off the Hard Drive the signal will change.

IMPORTANT NOTE: It is possible to get a harmonic of the proper DRUN display that looks correct but is not. Figure 3 shows what the **INCORRECT** DRUN signal may look like.

3. Error Amplifier adjustment.

This adjustment must be done during a continuous read. Since the DRUN adjustment does that, this adjustment should be done while the DRUN counter is running on the screen.

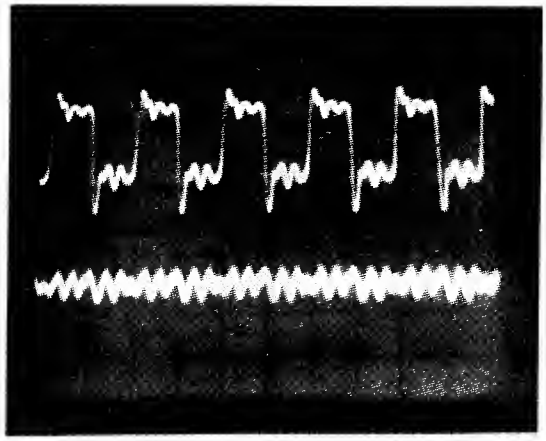
DC couple Channel A, set it to .5 volt/div. and connect it to TP8 again. TP8 is between the voltage regulator and U32. Set the time base to 2Ø microseconds/div. Set the trigger to normal and adjust the level control for a steady display.

Use R18 to minimize the pulses going up and down on the scope. They should be as small as possible and the positive and negative pulses should be about equal in size.

Once the above steps have been completed track 1 should be reformatted and the above procedure should be repeated until R18 and C33 do not require any further adjustment.

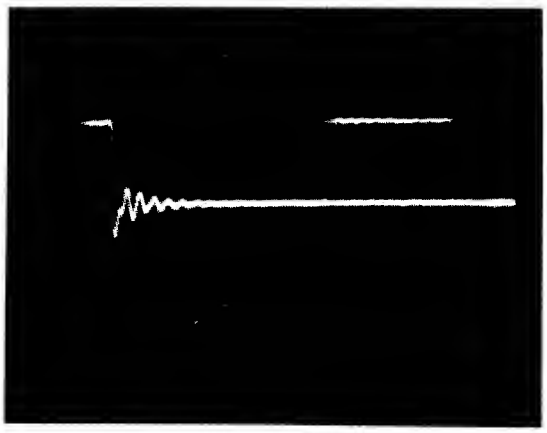
Channel A

Channel B



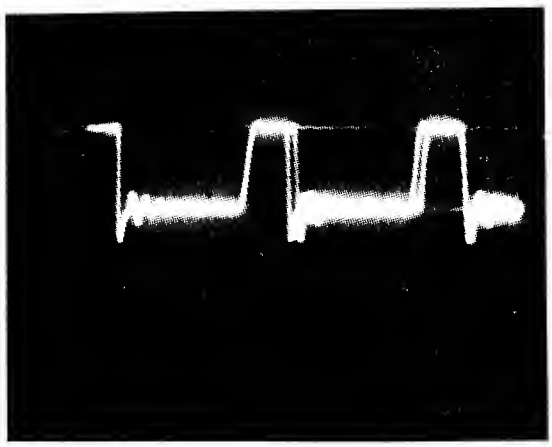
VCO
Channel A - TP9 2 volts/div.
Channel B - TP8 1 volt/div.
Time base - 5Ø nanoseconds/div.

Figure 1



DRUN
Channel A - TP1 2 volts/div.
Time Base - 5Ø nanoseconds/div.

Figure 2



INCORRECT DRUN

Figure 3

5 INCH HARD DISK ALIGNMENT PROCEDURE

For WD1Ø1Ø type boards

The hard disk controller board adjustments need to be done only on the primary hard drive. The motor speed will need to be adjusted on each hard drive in the system.

```
**************************************************
*                    WARNING                     *
*  This procedure should never need to be done.  *
*  C24 should only be adjusted if the waveforms  *
*          are obviously incorrect.              *
**************************************************
```

MINIMUM EQUIPMENT REQUIRED:

6Ø MHZ Oscilloscope (Tektronics 2213 or B&K 157Ø)
Plastic tunning tool
x1Ø scope probes

NOTE: 1. A MINIMUM 6Ø MHZ scope must be used.
2. DO NOT use a metal screwdriver for the adjustments as it can affect the circuit under test.
3. DO NOT use xl scope probes as they can load down the circuit under test.

1. VCO adjustment

Then attach Channel A of your scope to J5 pin 1 and set channel A to 2 volts/div.

DC couple Channel B, set it to 1 volt/div. and attach it to J5 pin 3.

The time base should be set for 5Ø nanoseconds/div., trigger should be normal and on channel A.

Adjust C24 to obtain exactly a 1ØØ nanosecond waveform on channel A and a +2.5 Vdc level on channel B. You should have your scope set up to display both of these signals at the same time. Adjusting one will affect the other. See Figure 1.

MODEL III RS-232-C DIAGNOSTIC TEST
RS232

CHAPTER 1Ø

TABLE OF CONTENTS

MODEL III RS-232-C DIAGNOSTIC TEST

General description

"RS232" is designed to allow thorough testing of the RS-232-C system of the TRS-8Ø Model III. Separate test functions are included to allow independent testing of the transmitter, receiver, UART, Baud Rate Generator, and interrupt circuits. When errors occur, error messages are displayed that will indicate the part of the system at fault.

Features

Complete menu driven test.
Auto, loop, and single test modes.
UART status, Baud Rate, and data words selectable by operator.

LOADING RS232 INTO THE COMPUTER

1. Power up the computer.
2. Boot the diskette.
3. When "TRSDOS READY" appears type: RS232 <ENTER>

MENU

The following menu will appear on the screen after Step 3 above:

TRS-8Ø MODEL III RS-232-C TEST

A AUTO TEST	U UART/BRG STATUS
L LOOP TEST	D T-R DATA TEST
E PE OR FE	M MODEM STATUS
I INTERRUPT	
X STOP/MENU	R LOAD UART
B TO BASIC	G LOAD BAUD RATE GENERATOR
S TO TRSDOS	H LOAD ONE-SHOT
	O T-R ONE-SHOT
	C DECODE TEST

QUICK REFERENCE/COMMAND DESCRIPTIONS

Each of the test routines will have the following features:

The operator will be required to attach a connector to the DB-25 connector that shorts pins 2 to 3, 4 to 5, and 6 to 8 to 2Ø.

If no error occurs a "PASSES TEST" message will be displayed.

If an error occurs an error message will be displayed and the auto test will end.

(A) AUTO TEST

The auto test will automatically perform the loop test at 8 different baud rates: 11Ø, 15Ø, 3ØØ, 6ØØ, 12ØØ, 24ØØ, 48ØØ, and 96ØØ. It will then check for parity errors, overrun errors, and framing errors. The interrupt circuits will be tested. The test will then start over and continue to run until another test is selected from the menu.

(L) LOOP TEST

The Loop Test will send and receive at preselected baud rate, each ASCII character, graphics character, and each special character in the Model III character set. The characters will be displayed on the screen one after the other until all have been received.

(E) PE OR FE

This checks the parity error, overrun error, and framing error circuits of the RS-232. Each of the error conditions are simulated and the test checks to make sure that the error flag is set. A check is also made to insure that the flag is not set on a no error condition.

(I) INTERRUPT

This routine tests the RS-232 interrupt vectors. This routine is heavily dependent on the integrity of the UART, Baud Rate Generator, ROM, and supervisory section of RAM. All other tests should be completed and verified before execution of this routine. The routine will disable all other interrupts except the specific RS-232 interrupts under test.

A single character will be transmitted using the interrupt drivers. If an interrupt does not occur within a specified time out period, an error will result. Also, an error is generated to test the error interrupt drivers along with other assorted logic.

(U) UART/BRG STATUS

This routine will display the status of the UART and Baud Rate Generator. Baud Rate, Word length, number of stop bits, and parity settings are displayed.

(D) T-R DATA TEST

This routine will display the status of the receiver and transmitter data registers from the last character transmitted or received. The condition of the Data Received, Parity error, Overrun error, and Framing error flags of the receiver section as well as each bit of the received word will be displayed. The condition of the Transmitter Holding Register flag and each bit of the transmitted word will also be displayed.

This routine is useful after errors occur in other routines. The status of the condition causing the error can be observed with this routine. For example, suppose during the Loop Test, an error message of "transmit and receive data mismatch" is displayed. Call the T-R Data Test and the actual transmitted word will be displayed with the received word and the bit causing the mismatch will be obvious.

(M) MODEM STATUS

This options allows the user to either test the RTS-CTS and DTR-DSR-CD signals or have the program automatically toggle the signals repeatedly for trouble shooting of the modem status lines using an oscilloscope. If a signal is bad, the test will display "Failed" and the status of the signal ("Stuck High" or "Stuck Low") for the Quick test. Use the toggle mode to pin-point the bad signal if this failure occurs.

(R) LOAD UART

This routine allows the operator to set the conditions of word length, stop bit size, and parity.

**********CAUTION**********

THE LOOP TEST AND AUTO TEST WILL INDICATE A FALSE ERROR IF THE UART IS PROGRAMMED TO A WORD LENGTH OTHER THAT 8 BITS.

(G) LOAD BAUD RATE GENERATOR

This routine allows the operator to set the baud rate to any of 8 different rates: 11Ø, 15Ø, 3ØØ, 6ØØ, 12ØØ, 24ØØ, 48ØØ, and 96ØØ.

After selecting the baud rate, the complete UART/BRG status will be displayed.

Any baud rate selected in the routine will be used in all other transmit/ receive routines except Auto Test.

(H) LOAD ONE-SHOT

This routine allows the operator to select two hex digits that will be used in a one-shot transmit/receive test. By selecting different hex digits any desired binary bit pattern can be tested.

(O) T-R ONE-SHOT

This routine will transmit and receive the word selected in the Load One-Shot routine. All error flags will be reviewed and error messages displayed as errors occur. The baud used will be that selected in the Load Baud Rate Generator option.

(C) DECODE TEST

This routine will cause the RS232 address decoder, U8, to send out low going strobes on each of its output pins. A message is displayed prompting the operator to connect an oscilloscope to the output pins of U8.

(X) STOP/MENU

This routine will return the operator to the master menu. It can be used during most other routines to stop the test and return to the main menu.

(B) TO BASIC

This routine will allow the operator to jump to Disk Basic in memory.

NOTE: Disk Basic must have been previously loaded into memory for this routine to function; if not, this routine will cause the program to appear locked-up. If a lock-up does occur, the Model III reset button must be pressed and RS232 loaded again.

(S) TO TRSDOS

This routine will allow the operator to return to TRSDOS. This routine would be useful for the operator to use other diagnostics after the completion of this series of test routines.

ERROR MESSAGES

The possible error messages are described in the following section. Some possible causes of these errors will be listed. These causes are not all inclusive.

PARITY(PE), OVERRUN(OE), AND FRAMING (FE) ERROR

A problem has been detected in the received data word. The T-R Data Test should be used to determine which error is present.

Possible cause: U2, U13, U7, U14 and U9.

TRANSMIT AND RECEIVE DATA MISMATCH

The transmitted data word and the received data word are not the same. The T-R Data Test should be used to look at the bit pattern of the transmitted data word and the received data word.

This type of error is caused by losing data bits between the transmit and received word. One possible cause is receiving a word longer than the word length set in the UART.

THRE NOT RESET AFTER LOAD

The Transmitter Holding Register Empty (THRE) flag did not change after a data word is loaded.

Probable cause: U2

FAILURE TO GIVE TRANSMIT INTERRUPT

The THRE flag from pin 22 of U2 did not cause an interrupt when an interrupt should have been detected.

Probable cause: U2, U14, U1Ø and U9.

FAILURE TO GIVE RECEIVE INTERRUPT

When a character was received in interrupt mode the Data Received (DR) flag on pin 19 of U8 did not cause an interrupt.

Probable cause: U2, U14, U1Ø, U9

FAILURE TO GIVE ERROR INTERRUPT

The three error conditions PE, OE, and/or FE from U8 did not cause an interrupt when an interrupt should have been generated.

FAILURE TO CLEAR RECEIVER REGISTER AFTER MASTER RESET

The Master Reset (MR) did not clear the Receiver Holding Register.

Probable cause: U18, U7, and U2

INTERRUPT DRIVEN TRANSMIT AND RECEIVE DATA MISMATCH

During the Interrupt test routine there was a mismatch between the transmitted word and the received word.

See the Transmitter and Receiver Data Mismatch error message above for probable causes.

PE, OE, FE NOT SET AFTER FORCED ERROR

A parity error, overrun error, or framing error was intentionally caused and the error was not detected.

Probable causes: U2, U27, U7, U14, U18 and U9

PE, OR, OR FE NOT SET AFTER FORCED ERROR INTERRUPT

The same as that above except that it should only occur during the Interrupt Test.

USR(UART STATUS REGISTER) CONTENTS INCORRECT AFTER MASTER RESET

After a master reset was sent to the UART, the UART USR (which contains the DR, OE, FE, PE, AND THRE flags) was incorrect.

Probable cause: U2

DR NOT RESET AFTER DATA RECEIVED

This error message means that the Data Received (DR) flag on pin 19 of U2 did not reset after data is received.

Probable cause: U2

TRANSMIT INTERRUPT NOT ACKNOWLEDGED

A transmit interrupt was generated but not acknowledged.

Probable cause: U9

RECEIVE INTERRUPT NOT ACKNOWLEDGED

A receive interrupt was generated but not acknowledged.

Probable cause: U9

DR NOT SET ON ERROR INTERRUPT

There was an receiver error generated in the interrupt driver test but the DR flag on pin 19 of U2 was not set.

Probable cause: U2

THRE NOT RESET AFTER TRANSMITTER INTERRUPT

During the interrupt test, the THRE flag on pin 22 of U2 was not reset.

Probable cause: U2

DEFINITIONS

RECEIVER REGISTER (RR)

The Receiver Register receives input data from pin 2Ø of U2 and stores it until a complete character has been received. The character is then transferred to the Receiver Holding Register.

RECEIVER HOLDING REGISTER (RHR)

The Receiver Holding Register will have the completed data byte transferred into it as soon as it has been processed by the Receiver Register.

The parallel contents of the Receiver Holding Register (RHR) appear on output lines RR1 - RR8 (pins 5-12 of the UART) when pin 4, the RRD input is at a logic low.

PARITY ERROR (PE)

If the receiver circuits detect an error between the count of high data bits and that preset in the UART status register parity bit and the even parity enable control sections, pin 13 of U2 will have a logic high level. This output is updated each time a character is transferred to the receiver holding register.

FRAMING ERROR (FE)

A logic high on output pin 14 of U2 indicates that the received character has no valid stop bit, i.e., the bit is not logic high following the data and parity bits. This output is updated each time a character is transferred into the receiver holding register.

OVERRUN ERROR (OE)

A logic high on output pin 15 of U2 indicates that the last character placed in the receiver holding register was not read by the CPU before the current character was received (and therefore was lost).

RECEIVER REGISTER CLOCK (RRC)

The receiver clock signal at a frequency of 16 times the selected baud rate is on pin 17 of U2. This frequency must be the same as the transmitter frequency for the device sending the data. It is possible for this frequency to be different from the transmission frequency of this UART. In the Model III this signal comes from the BRG, U1.

DATA RECEIVED RESET (DRR)

This input will transfer the parallel data from the RS232 to the main computer data bus and reset the UART for the next serial character.

A low logic level on pin 18 of U2 will reset the Data Received line. In the Model III RS232 board this active low will be sent in at the same time as the low on pin 4, the receiver register disconnect.

DATA RECEIVED

This signal indicates that a complete serial character has been received by the UART and is now in the RHR.

A logic high on pin 19 of U2 will occur when an entire serial character has been received and transferred to the receiver holding register. This line will be reset by a low on pin 18 as an acknowledgement by the computer that the parallel data has been transferred from the UART.

RECEIVED INPUT (RI)

This input is the serial data transmitted to the RS-232-C DB-25 connector.

Serial input data received on pin 2Ø of U2 enters the receiver register at a point determined by the character length, parity and number of stop bits. A high logic level must be present when data is not being received.

MASTER RESET (MR)

A logic high on pin 21 of U2 will reset the registers and error flags in the UART.

TRANSMITTER HOLDING REGISTER EMPTY (THRE)

This flag indicates that the transmitter is ready to accept a new character for serial encoding.

A logic high output level will be present on pin 22 of U2 to indicate that the Transmitter Holding Register has transferred its contents to the Transmitter Register and may be loaded with a new character.

TRANSMITTER HOLDING REGISTER LOAD (THRL)

This input to the UART will cause the contents of the CPU data bus to be loaded into the THR.

When parallel data from the computer data bus is to be loaded into the UART, a logic low on pin 23 will latch the character into the transmitter holding register. A transition from low to high transfers the data from the transmitter holding register into the transmitter register if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.

TRANSMITTER REGISTER OUTPUT (TRO)

The TRO is the serial output data containing the start bit, character data bits, parity bit, and stop bit(s).

The contents of the transmitter register including start bit, data bits, parity bit, and stop bit(s) are serially shifted out on pin 25 of U2. When no data is being transmitted, pin 25 will remain at a high logic level. Start of transmission is defined as the transition of the start bit from high to low.

TRANSMITTER REGISTER DATA (TR1 - TR8)

The TRD is the eight parallel data bus lines.

The eight data bus lines D0 - D7 are applied to pins 26 - 33 of U2. The data on these lines is loaded into the transmitter holding register by the pulse on pin 23. If an output character length of less than 8 bits has been selected, the character is right justified to the least significant bit, and the excess bits are disregarded. A logic high input on a data line will cause a logic high output on pin 25 at the time the bit is transmitted.

CONTROL REGISTER LOAD (CRL)

This signal will load the word size, parity set, and stop bit size information from the D3-D7 lines of the data bus.

A logic high input on pin 24 of U2 will load the control register bits with the logic level from pins 35 - 39. These inputs will be discussed individually in the following paragraphs.

PARITY INHIBIT (PI)

A logic high on pin 35 of U2 will cause the UART to inhibit the parity generation and verification circuits. Pin 13, Parity Error output will be clamped to a logic low. If parity is inhibited, the stop bit(s) will immediately follow the last data bit of transmission.

STOP BIT(S) SELECT (SBS)

Pin 36 of U2 is used to select the number of stop bits to be transmitted after the parity bit. A logic high on pin 36 will cause two stop bits to be included in the serial character, while a logic low will cause one stop bit to be included. If the word length selected is 5 bits and SDS is high, there will be 1 1/2 stop bits instead of 2 stop bits.

WORD LENGTH SELECT (WLS1 - WLS2)

Two input pins are used in binary format to select one of four possible serial word lenghts. Pins 37 and 38 of U2 can have any of the combination of logic highs or lows listed in the chart below to select from 5 to 8 data bits to be included in the output serial character.

PIN 37	PIN 38	WORD LENGTH
L	L	5 BITS
L	H	6 BITS
H	L	7 BITS
H	H	8 BITS

EVEN PARITY ENABLE (EPE)

Pin 39 is an input used to determine whether even or odd parity is to be generated by the transmitter and checked by the receiver. A logic high input selects even parity, while a logic low selects odd parity. If pin 35, parity inhibit input, is high, the logic level on the pin will be ignored.

TRANSMITTER REGISTER CLOCK (TRC)

The transmitter clock frequency of sixteen times the transmission baud rate is input on pin 4Ø of U2. This frequency is not necessarily the same as that of the receiver clock.

MEM4M & BD16K MEMORY TESTS

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MODEL 4/4P MEMORY TESTS

Introduction

The Model 4/4P Memory Tests are available in two versions to allow efficient testing of the various configurations of the Model 4/4P Computers. This allows the technician maximum flexibility in testing RAM, ROM, and Video Memory.

1. M4MEM/CMD — For Disk System Memory Tests (64K and 128K only)

2. BD16K/CMD — for cassette tape loading (16K only)

The only material required for these tests is an optional printer connector. See Appendix B for details on its construction.

Features

Tests Dynamic Ram, Video Ram, Rom, Sound board, and the printer port (optional) in the Model 4/4P Computers.

Tests data retention under wait states (refresh suspended) by utilizing wait states and the "waitimout" circuit on the FDC card (in disk systems only).

Advantages

Allows the technician to verify all memory in the Model 4/4P computer. Shows a "hour:minute:second" format on the screen to aid in identifying time related problems. Checks ROMS and displays checksums on each pass of the test. Checks dynamic and video RAM by a random pattern method.

LOADING AND EXECUTING M4MEM

In TRSDOS command mode type:

M4MEM <ENTER>

to execute M4MEM/CMD

LOADING AND EXECUTING BD16K/CMD

<<< THIS VERSION WILL NOT LOAD OR RUN WITH TRSDOS!! >>>

To use BD16K, it will first have to be transferred to cassette tape, since the 16K Model 4 will not support disk drives. See Appendix A for instructions on how to transfer and run BD16K.

To load and execute the tape version, enter BASIC (non-disk), prepare cassette, and type:
"SYSTEM <ENTER>"

At the "*?" prompt reply "BD16K <ENTER>"
At program will now load from cassette.

At the "*?" prompt reply "/ <ENTER>" to execute program.

DESCRIPTION OF TESTS

Both tests run in an identical manner. The first step of the test is to check the sound board. The test consists of a series of rising pitches, and simply gives a GO/NO GO type of test for the sound board. Next, the Real Time Clock interrupt storage locations are thoroughly checked to make sure that memory errors will not interfere with the operation of the timer function. Then the video/dynamic RAM tests are performed.

These tests will run continuously until the RESET key is pressed.

While the memory test is running, the top line of the display shows the results of several other system tests. A typical top line will look like the following:

16K: 6Ø HZ, ECH OK, LP OK, BBC4 DA75 4Ø7C 1591 ØØ:ØØ:ØØ 64K

This information is interpreted as follows:

16K — The memory size being tested. M4MEM will use this to display the memory bank correctly under test.

6Ø HZ — Indicates the video generator is set for a 6Ø HZ frame rate. If the VDG is set for a 5Ø HZ (European) frame rate, this line will indicate that fact.

ECH OK — Indicates the result of a test of port ØECH. Port FF allows the computer to read back the bits written to bits 1-5 of port ECH. A failure here indicates a problem in the addressing of either ports ØECH or ØFFH.

LP OK — Indicates the results of a line printer port test. This test requires a special printer port loop back connector (see appendix B) to run properly. If this connector is missing the display will show LP BAD.

BBC4 DA75 — Checksums for ROM A. Rom A is checked in two 4K segments with a separate checksum for each segment.

4Ø7C — Checksum for ROM B.

1591 — Checksum for ROM C.

ØØ:ØØ:ØØ — Elapsed time indicator.

64K — This line will show either 64k or 128k, depending on the amount of memory M4MEM finds installed in the computer.

ROM TEST

The first two 4 digit hexadecimal numbers from the left (BBC4 DA75) represent the checksum of the first ROM A. The next 4 digit hex number represents the checksum of ROM B. The next 4 digit hex number represents ROM C.

Current Valid ROM Checksums

ROM A	BBC4 DA75
	B5Ø4 DA42
	B523 DA42
ROM B	4Ø7C
ROM C early mfg. no 8ØØ4Ø316	1591
	48BC

**** NOTE ****

ROMS with slow access times may not be found faulty by this method of testing.

VIDEO/DYNAMIC RAM TEST

The memory test is accomplished as follows:

A random number is generated. This is stored in the first memory location to be tested. The memory address is incremented, as is the data byte. The next data byte is stored in the next memory location. This process is repeated until the data byte equals ØFEH.

When the data byte equals ØFEH, the data byte is changed to ØØH. The above process of increment data, increment memory, and store data is repeated until the memory is filled. The memory is then checked to verify that the correct data was stored in it. If all the memory checks OK then the process is repeated, with the data byte in all locations incremented by one. This accounts for the 'walking data' pattern on the screen.

Once the data pattern in the first memory location reaches ØFEH the program switches to the 'rotation' mode. Each memory location is now rotated one bit and checked. This rotation scheme is repeated eight times to check all eight bits. After the Rotation pattern is completed a new random number is generated and the entire process is repeated.

If a fault is found in video RAM the fault message may appear altered as a function of the failure. In this case compare the ASCII code you see with the correct code to determine which bits are incorrect.

BD16K/CMD

This version is incompatible with TRSDOS, and can only be loaded and executed from tape. This version does not test the memory for data retention with WAIT states as the other versions do, since that feature requires an FDC to be present in the machine.

MEM4M/CMD

The test is basically the same as BD16K/CMD except that the program will test the 2 millisecond dynamic RAM refresh specification by using the "waitimout" counter on the FDC board. This is accomplished by selecting the motor on signal to generate two 1 millisecond delays thus forcing the CPU into a 2 millisecond wait state. The drive motors will run for the first six minutes of each hour the test is run.

Troubleshooting Hints:

Difficult to locate or heat related problems may take several passes. To help detect heat related problems, hot or cold air may be applied during the tests.

It may require several hours to locate a fault affecting only one memory bit.

A binary sequence will test RAMS in the "low bit" positions more than in the "high bit" positions. Due to this property, it may be advantageous to exchange the RAMS in the "high side" positions (D4-D7) with those in the "low side" positions (DØ-D3), if a memory problem is suspected but not found in a reasonable period of time.

Random faulty bits or multiple chip failures may be an indication that the decoders, multiplexers, or buffers are causing problems.

The RAM banks should be visually examined to determine that all pins on all chips are in place and that the memory jumpers are in the correct positions. A check of +5, +12, and -5 volt power should also be made at that time.

NOTE: RAMS with improper voltages applied (i.e., - the five volt pin not inserted correctly) have been known to pass this test.

No one memory test is totally conclusive; therefore, use all the memory tests available in difficult situations.

APPENDIX

APPENDIX A

HOW TO TRANSFER BD16K/CMD TO TAPE

<<< THIS VERSION WILL NOT RUN OR LOAD WITH TRSDOS!! >>>

This version is supplied on diskette. IT IS NECESSARY TO TRANSFER THIS VERSION TO TAPE BEFORE USING! Use the TRSDOS "TAPE" command to transfer to cassette:

Connect the cassette recorder to Model 4 and set it to the RECORD mode with a blank cassette installed. Make sure the cassette is advanced past the leader.

In TRSDOS command mode type "TAPE (S=D,D=T) <ENTER>".

TRSDOS will prompt "CASS?".
Reply "H" for 15ØØ BAUD

TRSDOS will prompt "DEVICE = DEVICE TO TAPE - FILESPEC?"
Reply "BD16K/CMD <ENTER>"

"PRESS ANY KEY WHEN READY" will be displayed. Do so, and a tape copy will be written.

To load and execute the tape version, enter BASIC (non-disk!), prepare cassette, and type:
"SYSTEM <ENTER>"

At the "*?" prompt reply "BD16K <ENTER>"
At program will now load from cassette.

At the "*?" prompt reply "/ <ENTER>" to execute program.

APPENDIX B

PRINTER LOOPBACK CONNECTOR

Parts needed:

Printer edge card connector (Radio Shack cat. # 276-1564)
Wire wrap wire
Wire cutters
Soldering iron
Solder

Using the wire wrap wire, jumper the following pins on the printer interface connector:

Pin#	to	Pin#
3	--------	32
5	--------	3Ø
7	--------	29
9	--------	19
11	--------	28
13	--------	25
15	--------	23
17	--------	21

Check the connector for loose or broken wires and solder shorts. When using the connector, make sure that it is connected in the correct direction (EVEN pin towards the REAR of the Model 4).

Note that this connector and diagnostic program tests the four 'spare' data input lines. If one of the 'spare' lines is faulty it is possible for the printer port to work properly with a printer, but the diagnostic to give a 'LP BAD' message.

PRELIMINARY MODEL 4/4P TESTS

CHAPTER 12

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INTRODUCTION

The Preliminary Model 4 Diagnostics contains the programs necessary to fully check the TRS-8Ø Model 4 Microcomputer or the Model 4 upgrade kit for the Model III Microcomputer. Included are two video tests and two system tests.

Although these tests are supplied on a Model III TRSDOS 1.3 diskette, the Model 4 Diagnostic programs were designed to test the many features of the Model 4 Microcomputer. In most cases these tests will not function on the Model III.

Most of the Model 4 Diagnostic programs are self prompting, or contain an operational menu which appears on the screen. Still some discussion of these tests may prove helpful. The following pages contain these discussions.

VIDEO TESTS

There are two video tests on the Model 4 Diagnostics diskette. The first is a Video Alignment Pattern (VAP/CMD). The second is a basic function test (VIDD/BAS).

VAP/CMD

Entering 'VAP' at the TRSDOS READY prompt will produce an 8Ø X 24 Video Alignment pattern to be used to align the video PCB and CRT. All lines should appear straight, the display should not appear rotated, and the screen should be in focus over its entire area. If necessary, corrections should be made to the video PCB controls or to the CRT and yoke.

Press RESET to exit this test.

VIDD/BAS

VIDD/BAS is a test, written in BASIC to test the different screen display modes of the Model 4. To run the program, at TRSDOS READY type 'BASIC VIDD/BAS' and then press the ENTER key.

When the program loads and runs it will appear to 'lock up' at first. This is normal. Be patient.

After a short time the MENU will appear. There are 1Ø tests available. A discussion of each follows.

32, 4Ø, 64, and 8Ø CHARACTER TESTS

The 32, 4Ø, 64, and 8Ø character tests simply demonstrate the Model 4's ability to produce both normal and double width characters in both 64x16 and 8Øx24 character modes.

PAGE TEST

The PAGE test demonstrates the paging feature of the video memory. In the 64 character mode the video memory is treated as two pages of 1K bytes each. Two sets of figures should be seen during this test, indicating the ability to properly access both pages. The display is in the 8Ø character mode so that both pages may be displayed on the screen at the same time.

FAST TEST

FAST exercises the high speed clock ability of the Model 4. The most obvious test would be to check the processor clock itself, but this is only part of the story. Going into the high speed mode also changes the Real Time Clock interrupt rate to 60HZ rather than the 30HZ of the slow rate. The visible increase in the timer rate is due to the increase in the interrupt rate, and not because the processor clock is running faster.

ALTERNATE CHARACTER TEST

The ALTERNATE CHARACTER TEST demonstrates the alternate characters available from the character generator ROM.

INVERSE VIDEO TEST

The INVERSE VIDEO TEST shows the inverse video characteristics of the Model 4.

MOVING VIDEO TEST

The MOVING VIDEO TEST shows the VDG's ability to access the total 2048 bytes of video RAM. While 2048 bytes of video RAM are supplied, only a maximum of 1920 bytes are used by the 80x24 mode, leaving 128 bytes unused. The moving video test adjusts the VDG addresses so that these last 128 bytes are displayed. This checks for RAM failures in the last 128 bytes, and also checks the VDG's ability to access this section of video RAM.

KEYBOARD TEST

The KEYBOARD TEST tests the extra function keys available to the Model 4.

SYSTEM TESTS

MIVKEY/CMD

MIVKEY is a machine level program that is run from TRSDOS READY. It contains an explanation/instruction page of its own.

The purpose of MIVKEY is to relocate the ROM into RAM, and to "relocate" the keyboard into high memory. In this mode the ROM code can now be changed, demonstrated by the 'Model IV Basic' message.

Note that although the display is 80x24, the BASIC interpreter ROMs (now in RAM) still expect a 64x16 display, making LIST's and PRINT@'s appear odd.

This mode of operation also demonstrates the Model 4's ability to become CP/M compatible.

END

END is a BASIC program. To run it, type 'BASIC END' from the TRSDOS READY prompt.

This program contains its own menu and is self explanatory. It contains a 500 and 1500 baud cassette test, a printer test (a printer must be attached and turned on), a video alignment pattern, a displayable character test, a BASIC functions test, and a disk functions test which can be used if disks are available.

END will have to be transferred to tape before it can be run on a 16K Model 4. On Early versions of the program, the cassette tests will not work on a 16K computer. Since this is a BASIC program, the procedure will not be discussed here.

PLOAD

CHAPTER 13

PLOAD
Down-load Program For the Model 4A/4P

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PLOAD/CMD - DOWN-LOAD PROGRAM FOR THE MODEL 4P

GENERAL DESCRIPTION

"PLOAD" is designed to allow downloading of programs from a Model III/4 to a Model 4P without using the Model 4P's floppy drives. "PLOAD" uses the Model 4P's ability to boot from the RS-232 interface to download programs. "PRCV" is the companion program that is first downloaded to the Model 4P. "PRCV" receives the programs sent by "PLOAD" and loads them into the Model 4P's memory. If the Model III ROM Image is being downloaded, "PRVC" will load it into the appropriate memory location and then set the 4P's memory map to write-protect that area of memory. The desired program is then downloaded and executed.

FEATURES

Six selectable baud rates.
Model III ROM Image may be downloaded.
Generous prompting to prevent errors.

EQUIPMENT REQUIRED

TRS-8Ø Model III/4 (source computer).
TRS-8Ø Model 4P (destination computer).
2 RS-232 cables with DB-25 connectors.
Nul-Modem adapter.
"PLOAD/CMD" download program.
"PRCV/CMD" Model 4P RS-232 receive program.
"MODEL/III" Model III/4 ROM Image file.

QUICK REFERENCE

1. Connect the RS-232 port on a Model III/4 to the RS-232 port on the Model 4P using a null-modem adapter.
2. Turn on and boot the Model 4.
3. Turn on the Model 4P holding the right SHIFT key down until either "Not Ready" or "Ready" appear.
4. Run "PLOAD/CMD" on the Model III/4.
5. Enter the full filename at the filename prompt.
6. Select appropriate baud rate.
7. Press <Y> in response to next two prompts.
8. Check for blinking asterisk in top right corner of Model 4P.

TECHNICAL SECTION

LOADING "PLOAD/CMD"

1. Connect the RS-232 ports on the Model III/4 and the Model 4P using the null-modem adapter.
2. Power up the Model III/4.
3. Power up the Model 4P and hold down the right SHIFT key until either a "Not Ready" or "Ready" message appears. "Not Ready" indicates that the host (the Model III/4) has not asserted Data Terminal Ready. "PLOAD" enables the RS-232C and causes DTR to be asserted after all the prompts for "PLOAD" have been answered. Either message is acceptable.
4. When either the "Not Ready" or the "Ready" message appears on the Model 4P, release the right SHIFT key. If another message other than "Not Ready" or "Ready" should appear, press RESET on the Model 4P while holding the right SHIFT key down.
5. Boot the Model III/4 and type in PLOAD <ENTER>.

NOTE - If the 4P is powered up before the host computer, the 4P may lock up at "Ready". In this case, reset the 4P holding down the right SHIFT key.

OPERATING "PLOAD"

"PLOAD" is completely menu driven and contains no "hidden" commands. This means that you will not need to refer to the operations manual once you become familiar with the program!

All keyboard entries by the technician are made with CAPITAL letters. The Model III/4 defaults to an all caps mode. If for some reason the computer is in lowercase mode (no capital letters), on the Model III press <SHIFT> 0. On the Model 4, press the CAPS key.

OPERATION

When "PLOAD" finishes loading the menu page will appear on the screen. This menu will remain on screen at all times.

The Menu consists of a title block at the top and a prompt for a filename. The filename must be in the form filename/ext.password. All files that might be downloaded should have the default password of "PASSWORD" and the .password portion may be omitted. However, most files will have an extension such as /CMD and the extension must be included. There is no default extension. Type in the full filename including extension if any (e.g. TDC/CMD) and press <ENTER>.

"PRCV/CMD"

Once "PRCV/CMD" has loaded into the Model 4P, a title block similar to the one on the Model III/4 should appear. Below that block will be a message "Waiting for sync bytes from host". Once "PRCV" has synched with the host (Model III/4) the message "Sync received, loading file" will appear. As the file is loaded, a blinking asterisk will appear in the top right corner of the Model 4P's screen.

After loading the selected file, another awaiting sync message will appear, followed by "Sync received, loading ROM Image". The 4P is now receiving the MODEL/III ROM Image file. Once that file has been loaded, "PRCV" will re-map the 4P's memory to write-protect the area in which the ROM Image resides.

After loading the ROM Image, the program that was selected for downloading will be executed. If at any time a lock-up in the program should occur, try pressing the reset switch on the Model 4P. In most cases, the program should restart.